COMPUTE

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A PROM Programmer for the SC/MP LCDS

Application Note AN-189
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ABSTRACT

This application note describes for the user of the SC/MP Low Cost Development System (LCDS) a method of programming MM5204 or MM4204 Programmable Read Only Memories (PROMs) that is both inexpensive and highly efficient.

INTRODUCTION

In the development cycle, there is a point in software development between read/write memory program debug and commitment to mask programmed ROMs. This is generally filled by using erasable PROMs; this allows the user to test the program in the end application, and then to correct any errors that occur. Also, for the small quantity user, in the end application PROMs may be more practical to use instead of ROMs. This can be inconvenient, however, if a PROM programmer is not readily available.

With the method described in this application note, the LCDS user can construct, using wire-wrap techniques, an inexpensive PROM programmer that plugs into the SC/MP LCDS backplane and programs a 512-by-8 PROM in less than 10 seconds. The only additional item required is a 65 V power supply capable of delivering 500 mA.

CAPABILITIES

The driver software has the ability to copy a PROM into memory for subsequent duplication, to verify a PROM against memory, to program a PROM from any memory area, and to verify that a PROM is erased.

An added feature of the PROM programmer is an LED that is active when the high voltage is being applied to the PROM socket.

NOTE

Damage to the PROM and/or the programmer may result if the PROM is inserted or removed when the LED is turned on.

Listed at the end of this article are two versions of the driver software. If the user has a Teletype®, the first program can be used. If no Teletype is available, the second program uses the LCDS control panel for all entries.

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EXAMPLES OF TELETYPE OPERATION

The Teletype (TTY) program works in conjunction with the TTY DEBUG package contained on the LCDS Motherboard. The following are some examples of TTY operational routines; the user's read/write memory is assumed to be located from X'1000 to X'17FF.

NOTE

The 65 V power supply should be turned on throughout all of the following operations.

(A dash [-] denotes a debug prompt, a question mark [?] denotes a programmer prompt.)

Loading an LM Tape and Programming

-L1000 CR (CR = carriage return)	Load tape into memory starting at address X'1000.
-G0 CR	After tape loads, the user transfers to programmer software.
?P1000 CR	Check PROM for erased condition, then program from X'1000.
?V1000 CR	Verify PROM against memory.
?	Ready for next command.

NOTE

The PROM is now programmed. Pressing the HALT button returns to the DEBUG monitor if desired. The following examples show the initial system state to be in DEBUG.

Duplicating a PROM

-G0 CR	Transfer to programmer routines.
	Put PROM to be duplicated in socket on programmer card.
?C1000 CR	Copy PROM data into memory starting at X'1000.
	Put blank PROM in socket.
?P1000 CR	Program PROM.
?V1000 CR	Verify PROM.
?	Ready for next command.

Program PROM Without Check for Erased Condition

-G0 CR	Transfer to programmer routines.
	Put PROM in socket.
?Y1000 CR	Program PROM from X'1000 without check for erased.
?V1000 CR	Verify PROM.
?	Ready for next command.

Checking PROM for Erased Condition

-G0 CR	Transfer to programmer routines.
	Put PROM in socket.
?E	PROM is checked.
?	Ready for next command.

Listing Contents of a PROM

-G0 CR	Transfer to programmer routines.
	Put PROM in socket.
?C1000 CR	Copy PROM contents into memory.
	Press HALT button to transfer to DEBUG routines.
-T1000:11FF CR	Type contents of buffer area.

Error Messages

If PROM cannot be programmed:

?P1000 CR
BAD PROM @0XXX — where 0XXX denotes the address of the PROM that cannot be programmed

If PROM is not erased:

?P1000 CR
NOT ERASED

or

?E
NOT ERASED

If PROM does not verify against memory:

?V1000 CR
NO VERIFY

EXAMPLES OF PANEL OPERATION

For panel operation, the user enters the starting address of the routine to be executed into the Program Counter and the address to be used for copying, verifying against, or programming from into Pointer 1. After placing the PROM in the socket, the RUN button is pressed. The system halts when the operation is completed or if an error is detected. The error halts and their explanations follow:

X'0035	PROM is not erased.
X'0085	PROM cannot be programmed.
X'015A	PROM does not verify.

The following are entry points:

X'0001	Check PROM for erased condition.
X'0035	Program PROM without check for erased.
X'0048	Program PROM with check for erased.
X'0101	Copy PROM into memory.
X'012C	Verify PROM against memory.

When using the panel program, the HALT INST switch on the LCDS Motherboard must be in the DEBUG position before execution. Other than the method of inputting commands and parameters, the TTY program and PANEL program are functionally identical.

Generalized flowcharts of the PROM programmer software routines follow the listings.

These programs are intended to be assembled at X'0000 so they can be placed in PROM on the SC/MP CPU card. For the P-channel card, an MM5204 is used. On the N-channel card, an 87S296 bipolar PROM must be used. If N-channel is used, the delay constants in the programming routines must be doubled to allow the correct timing for the programming pulses.

BOARD CONSTRUCTION

Referring to the schematic diagram, figures 1 and 2, standard wire-wrap techniques are used in the construction of the board. Refer to photo 1 for a suggested placement layout. This placement should be followed as closely as possible, as the transistor drivers and their associated passive components should be near the PROM socket to reduce line inductance. The decoding and control circuits are placed near the board edge connector for access to the data and address buses.

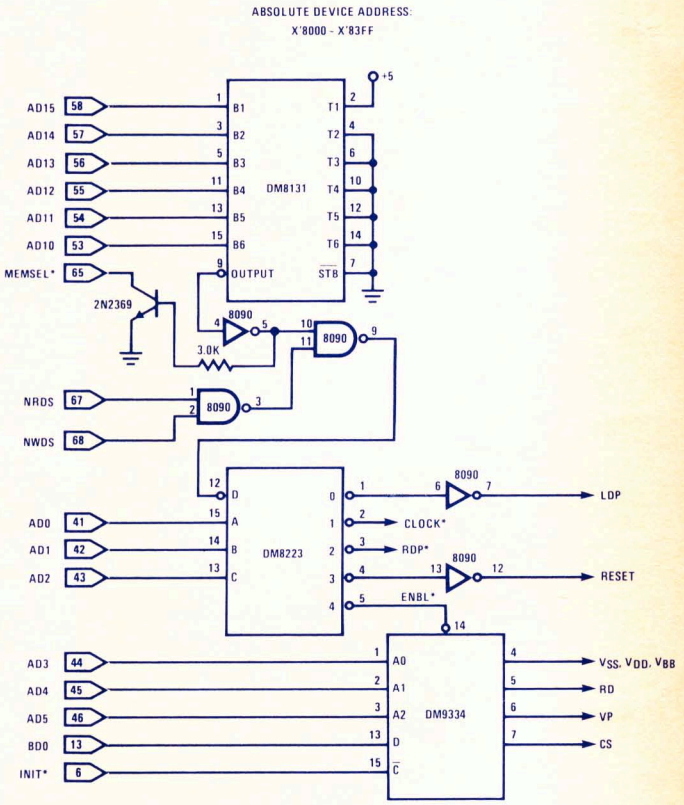

Figure 1.

It is suggested that a low or zero insertion force socket be used for the PROM to make insertion and removal easier. This also reduces the possibility of bent pins which can cause errors in programming or damage to the part.

Three waveform photos are included to aid in verification and debug of the circuit. Photo 2 shows the programming pulse from the DM9334 addressable latch and at pin 4 of the PROM. Photo 3 shows the voltage levels of input data for both the logic "0" and logic "1" states. Photo 4 shows the levels of V_{BB} and V_{DD}. All these values are shown during the time of the programming pulse.

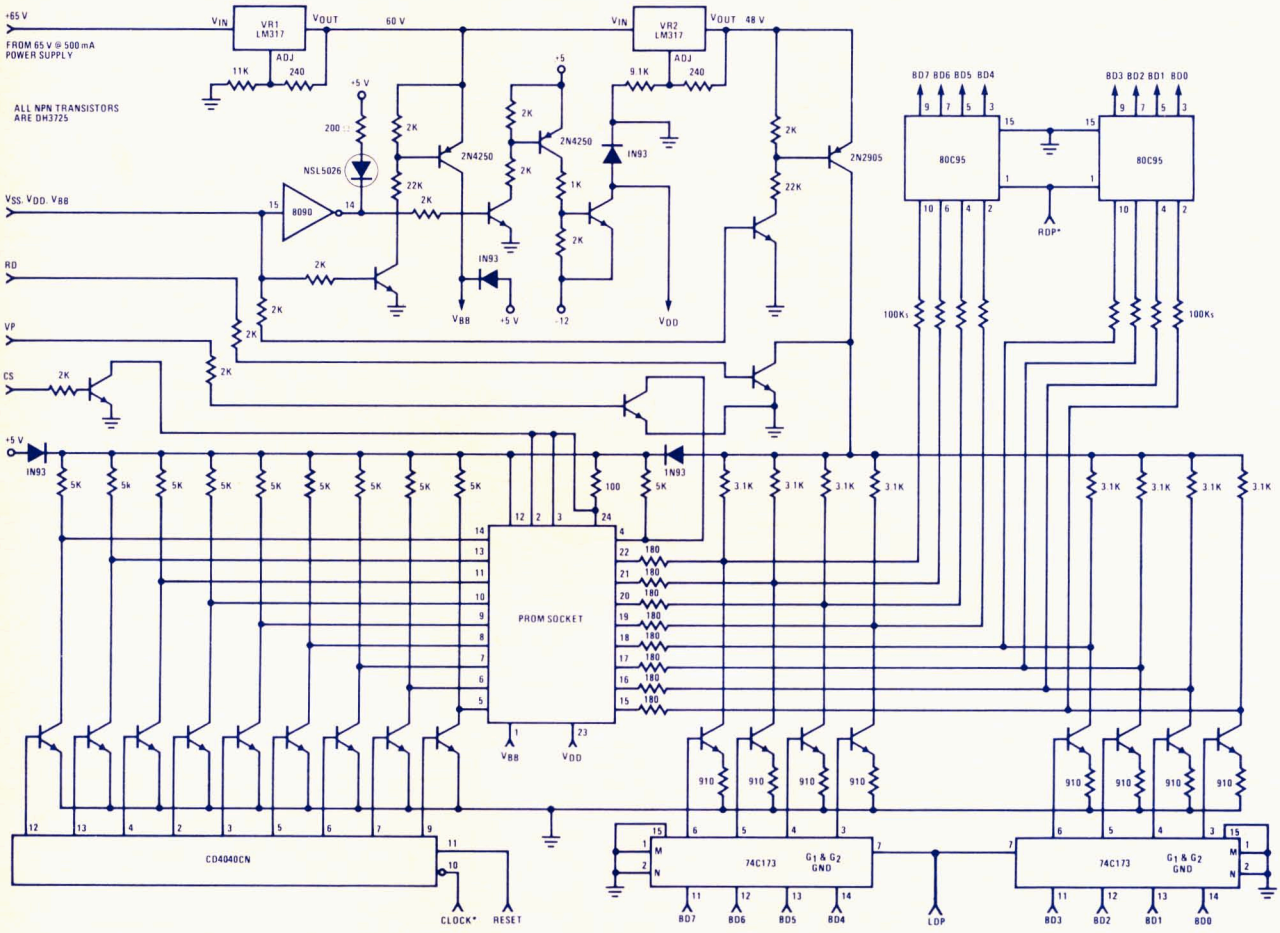

Figure 2.

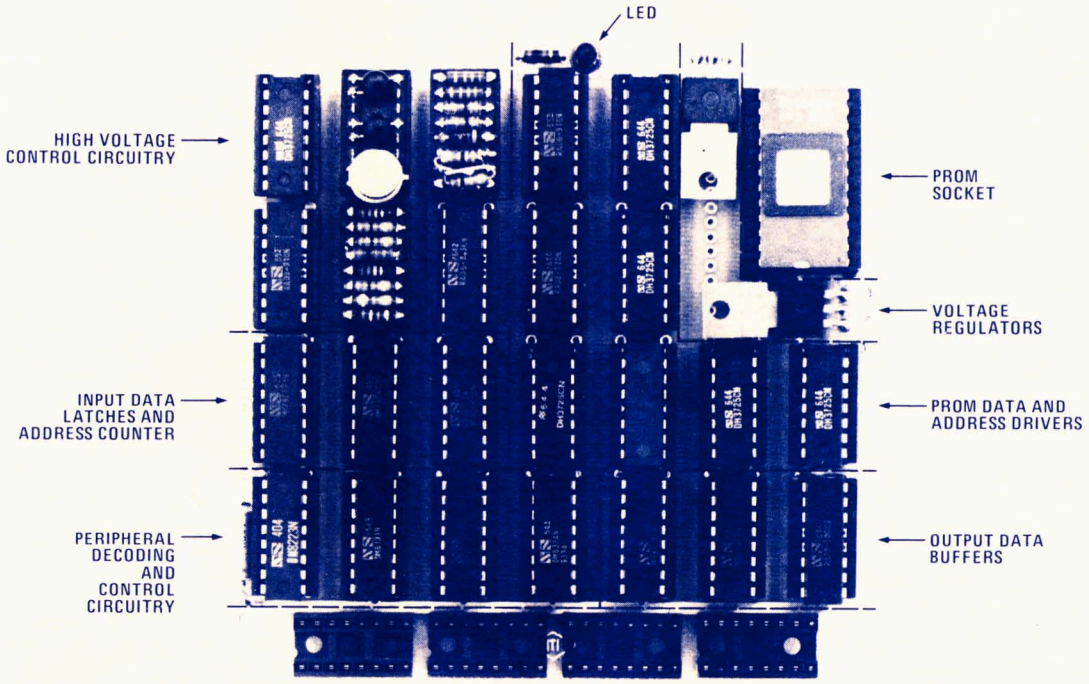

Photo 1.

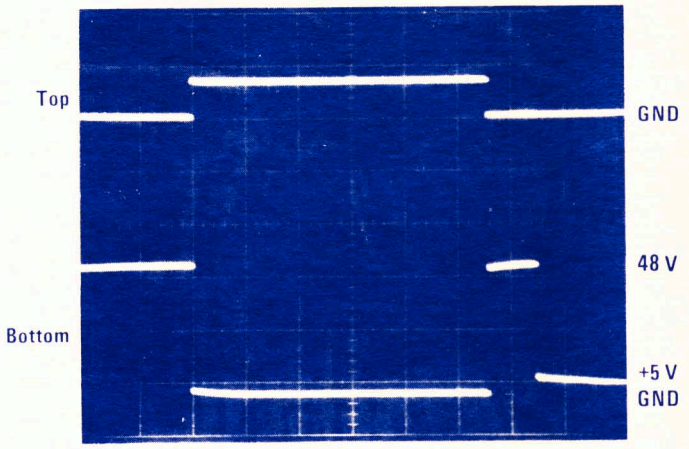

Photo 2. top: Vp @ 5 V/DIV & 200 μs/DIV
bottom: Vp (PROM) @ 20 V/DIV & 200 μs/DIV

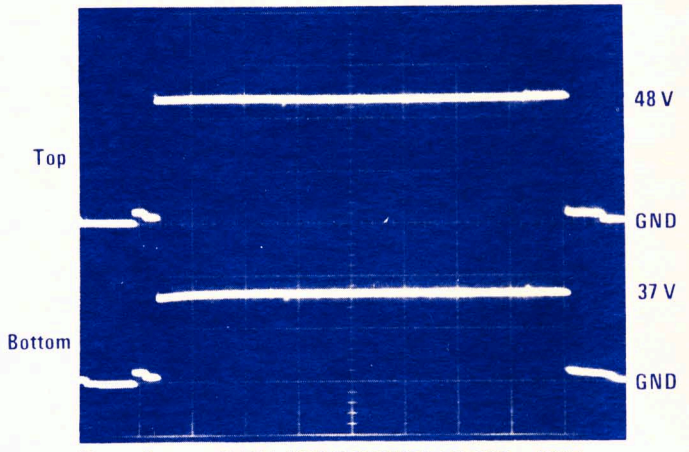

Photo 3. top: DATA "0" @ 20 V/DIV & 300 μs/DIV
bottom: DATA "1" @ 20 V/DIV & 300 μs/DIV

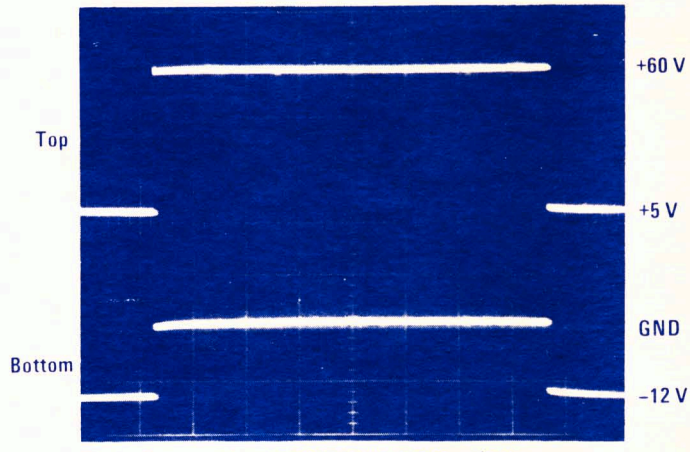

Photo 4. top: V_{BB} @ 20 V/DIV & 300 μs/DIV
bottom: V_{DD} @ 10 V/DIV & 300 μs/DIV

A suggested board for construction is National Semiconductor part no. IPC-16C/801 prototyping board. However, any prototype board that has a 72-pin edge connector on 0.100 inch centers (plug compatible with the SC/MP LCDS bus) and room for at least 32 16-pin IC sockets can be substituted.

Each TTL and CMOS circuit should be bypassed by a 0.1 μF capacitor across V_{CC} and GND as well as bulk capacitors across V_{CC} and GND and −12 V and GND at the input to the board. These capacitors should be tantalum and should be in the 20 μF to 30 μF range.

PARTS LIST

Type	Description	Quantity
DH3725CN	Quad Core Drivers	6
MM74C173	Quad Latch	2
DM80C95N	Hex Tri-State Buffer	2
CD4040N	12-Stage Binary Counter	1
DM8223N	1-of-8 Decoder	1
DM8131N	6-Bit Bus Comparator	1
DM8090N	Miscellaneous Gates	1
DM9334N	Addressable Latch	1
NSL5026	LED	1
2N4250	PNP Transistor	2
2N2905	PNP Transistor	1
1N93	Germanium Diode	4
LM317T	Voltage Regulator	2
RESISTORS	May be Resistor Arrays	62

CONCLUSIONS

This PROM programmer greatly extends the use of the SC/MP LCDS as a prototyping/development system by giving the user the ability to program PROMs for debug and test purposes while remaining much less expensive than commercially available PROM programmers. Also, since it is to be used in the LCDS, no special formats for the data are required. Load modules created by the SC/MP LCDS can be loaded by the firmware provided without conversion to binary, complemented binary, or BPNF formats.

```
                TITLE  'TTYPGM,  SC/MP PROM PROGRAMMER'

;  "TTYPGM" IS A PROGRAM THAT ALLOWS THE SC/MP
;  LCDS TO PROGRAM MM5204 OR MM4204 PROMS.

;  THE COMMANDS AND THEIR FORMATS ARE

;       CXXXX        COPY PROM INTO MEMORY

;       VXXXX        VERIFY PROM AGAINST MEMORY

;       E            VERIFY PROM IS ERASED

;       PXXXX        PROGRAM PROM FROM MEMORY
;                    WITH CHECK FOR ERASED

;       YXXXX        PROGRAM PROM FROM MEMORY
;                    WITHOUT CHECK FOR ERASED

;  WHERE XXXX IS THE HEX STARTING ADDRESS TO BE
;  USED.

;  THE PROGRAM REQUIRES THAT THERE ARE 512
;  CONTINUOUS MEMORY LOCATIONS UPWARDS FROM XXXX.

;  "TTYPGM" USES MEMORY ON THE LCDS MOTHERBOARD FOR
;  TEMPORARY STORAGE.  THEREFORE, USER R/W MEMORY
;  CAN BE ANYWHERE, EXCEPT AS SHOWN BELOW.

;  "TTYPGM" CAN BE ASSEMBLED ANYWHERE THE USER HAS
;  MEMORY SPACE EXCEPT IN THE FOLLOWING LOCATIONS:

;     X 8000 -- X 83FF       LOCATIONS OCCUPIED BY
;                            PROGRAMMER HARDWARE
;     X 7000 -- X 7FFF       LOCATIONS USED BY LCDS

;  A TELETYPE IS REQUIRED FOR EXECUTION.

                PAGE    POINTERS AND CONSTANTS

                =0

0001    P1      =       1
0002    P2      =       2
0003    P3      =       3

8000    PRGMR   =       08000       ;PERIPHERAL ADDR  OF PROM
                ;                   ; PROGRAMMER BOARD
0014    VP      =       014         ;ORDER CODE FOR PROG VOLTAGE
0000    RD      =       00          ;ORDER CODE FOR READ
0004    VSS     =       04          ;ORDER CODE FOR VSS,VBB,VDD
001C    CS      =       01C         ;ORDER CODE FOR CHIP SELECT
0008    LOAD    =       8           ;ORDER CODE TO LOAD DATA
0001    CTR     =       1           ;ORDER CODE TO CLOCK COUNTER
0002    RDPRM   =       2           ;ORDER CODE TO READ PROM
                ;                   ; DATA
```

```
                CLR     =       3               ;ORDER CODE TO CLEAR COUNTER
                ENBL    =       4               ;ORDER CODE TO ENABLE CONTROL
                                                ; LATCH
                PUTC    =       07AF2           ;PUT CHARACTER POINTER
                GECHO   =       07A91           ;GET CHARACTER W/ECHO POINTER
                GHEX    =       07B50           ;POINTER TO GET 4 HEX DIGITS
                MESG    =       07B17           ;POINTER TO MESSAGE ROUTINE
                PHEX    =       07BB3           ;POINTER TO PUT HEX ROUTINE
                STACK   =       077D0           ;STACK POINTER TO MOTHER-
                                                ; BOARD R/W MEMORY
                HI      =       -17             ;TEMPORARY LOCATIONS OFFSET
                LO      =       -18             ; FROM STACK POINTER
                SAVLO   =       -19
                SAVHI   =       -20
                HCNT    =       -21
                DPLO    =       -22
                DPHI    =       -23

                        PAGE    'COMMAND INPUT PROCESSING'

                ; COMMAND ENTRY ROUTINE

0000 08                 NOP
                ENTRY
0001 C477               LDI     H(STACK)        ;INITIALIZE STACK PTR
0003 36                 XPAH    P2
0004 C4D0               LDI     L(STACK)
0006 32                 XPAL    P2
                PROMPT
0007 C47B               JS      P3,MESG         ;PROMPT FOR COMMAND
0009 3714
000B 1633
000D 3F
000E 01EC                DBYTE PRMPT
0010 C47A               JS      P3,GECHO        ;GO TO GET CHAR W/ECHO
0012 37C4
0014 9033
0016 3F
0017 047F               ANI     07F             ;MASK OUT PARITY, IF ANY
0019 01                 XAE                     ;SAVE CHAR IN E REG
001A C401               LDI     H(CMDTBL)       ;SET PTR TO COMMAND TABLE
001C 35                 XPAH    P1
001D C4F0               LDI     L(CMDTBL)
001F 31                 XPAL    P1
0020 02                 CCL
                CLOOP
0021 F503               LD      @3(P1)          ;GET COMMAND CHAR
0023 980E               JZ      ERROR           ;END OF TABLE, INPUT ERROR
0025 60                 XRE                     ;CHECK FOR CORRECT COMMAND
0026 9CF9               JNZ     CLOOP           ;NOT RIGHT, TRY NEXT
0028 C5FF               LD      @-1(P1)         ;FOUND COMMAND, GET ADDR
002A 01                 XAE                     ;SAVE TEMPORARILY IN E REG
002B C5FF               LD      @-1(P1)
002D 35                 XPAH    P1
002E 40                 LDE
002F 31                 XPAL    P1
0030 3D                 XPPC    P1              ;EXECUTE COMMAND
0031 90D4               JMP     PROMPT
                ERROR
0033 C4E1               LDI     L(PUTC)-1
0035 33                 XPAL    P3
0036 C43F               LDI     '?'
0038 3F                 XPPC    P3
0039 90CC               JMP     PROMPT

                        PAGE    'PROM ACCESS AND PROGRAMMING ROUTINES'

                ; ROUTINE TO CHECK PROM FOR ERASED CONDITION

                ; THIS SUBROUTINE IS ALSO CALLED BY "PROG " TO VERIFY
                ; THAT THE PROM IS ERASED

                ERASED
003B C480               LDI     H(PPRGMR)       ;SET ADDR OF PROGRAMMER
003D 37                 XPAH    P3
003E C400               LDI     L(PPRGMR)
0040 33                 XPAL    P3
0041 C401               LDI     1               ;SET UPPER COUNT
0043 CAEF               ST      HI(P2)          ;STACK IS EMPTY, USE AS PTR
0045 CB0C               ST      RD(P3)          ;SET READ MODE
0047 CB1C               ST      CS(P3)          ;SELECT PROM SOCKET
0049 C400               LDI     0               ;SET LOWER COUNT
004B CAEF               ST      LO(P2)
004D CB03               ST      CLR(P3)         ;CLEAR PROM COUNTER
004F CB00               ST      LOAD(P3)        ;CLEAR DATA LATCHES FOR
                ELOOP                           ;READ
0051 C302               LD      RDPRM(P3)       ;READ DATA OUT OF PROM
0053 9C0B               JNZ     NOT             ;DATA NOT ZERO? NOT ERASED
0055 CB01               ST      CLK(P3)         ;DATA OK, BUMP COUNTER
0057 BAEF               DLD     LO(P2)          ;DECREMENT LOWER COUNT
0059 9CFA               JNZ     ELOOP           ;NOT DONE YET
005B BAEF               DLD     HI(P2)          ;DECREMENT UPPER COUNT
005D 94F2               JP      ELOOP           ;NOT DONE YET
005F 3D                 XPPC    P1              ;PROM IS ERASED
                NOT
0060 C47B               JS      P3,MESG         ;GO TO MESSAGE RTN
0062 37C4
0064 1633
0066 3F
0067 01C4                DBYTE NOTMSG           ;PTR TO MESSAGE
                RETN2
0069 909C               JMP     PROMPT          ;RETURN TO COMMAND PROCESS

                ; ENTRY POINT TO PROGRAM PROM W/O CHECK FOR ERASED

                WOCHK
006B C47B               JS      P3,GHEX         ;GET ADDR TO PROG FROM
006D 37C4
006F 4F33
0071 3F
0072 C480               LDI     H(PPRGMR)
0074 37                 XPAH    P3
0075 C400               LDI     L(PPRGMR)
0077 33                 XPAL    P3
0078 C601               LD      @1(P2)          ;GET UPPER BYTE OF ADDR
007A F402               ADI     2               ;ADD 512 OFFSET
007C 35                 XPAH    P1
007D C601               LD      @1(P2)          ;GET LOWER BYTE
0080 901D               JMP     SET

                ; ENTRY POINT TO PROGRAM PROM W/CHECK FOR ERASED

                ; PROM IS PROGRAMMED FROM MOST SIGNIFICANT ADDRESS TO
                ; LEAST SIGNIFICANT ADDRESS DUE TO COUNTER INVERSION

                PROG
0082 C47B               JS      P3,GHEX         ;GET ADDR TO PROGRAM FROM
0084 37C4
0086 4F33
0088 3F
0089 C601               LD      @1(P2)          ;RETRIEVE ADDR FROM STACK
008B 01                 XAE
008C C601               LD      @1(P2)
008E CAED               ST      SAVLO(P2)       ;SAVE IN R/W MEMORY
0090 40                 LDE
0091 CAEC               ST      SAVHI(P2)
0093 C43A               LDI     L(ERASED)-1     ;CHECK PROM FOR ERASED
0095 31                 XPAL    P1
0096 3D                 XPPC    P1
0097 C2ED               LD      SAVLO(P2)
0099 31                 XPAL    P1
009A C2EC               LD      SAVHI(P2)
009C F402               ADI     2               ;ADD 512 OFFSET
009E 35                 XPAH    P1
009F C401       SET     LDI     1
00A1 CAEF               ST      HI(P2)          ;SET UPPER LOC COUNT
00A3 C400               LDI     0
00A5 CAEE               ST      LO(P2)          ;SET LOWER LOC COUNT
00A7 CB03               ST      CLR(P3)         ;CLEAR PROM COUNTER
                NXTLOC
00A9 C5FF               LD      @-1(P1)         ;GET DATA TO PROGRAM
00AB 01                 XAE                     ;SAVE IN EXTENSION REG
                THSLOC
00AC C401               LDI     H(PPROM)        ;SET ADDR OF PROGRAMM RTN
00AE 35                 XPAH    P1
00AF CAEC               ST      SAVHI(P2)       ;SAVE PTR ADDR
00B1 C421               LDI     L(PPROM)-1
00B3 31                 XPAL    P1
00B4 CAED               ST      SAVLO(P2)
00B6 C4FF               LDI     -2              ;SET COUNT
00B8 CAEB               ST      HCNT(P2)        ;SAVE HIT COUNT IN RAM
                GO
00BA 3D                 XPPC    P1
00BB 60                 XRE                     ;CHECK PROM DATA
00BC 981B               JZ      OK              ;PROM DATA CORRECT, DO X+5X
00BE BAEB               DLD     HCNT(P2)        ;DECREMENT HIT COUNT
00C0 9CF8               JNZ     GO              ;CHECK FOR MAX. HIT
                NPROG
00C2 C47B               JS      P3,MESG         ;HIT COUNT OVER MAX, BAD PROM
00C4 37C4
00C6 1633
00C8 3F
00C9 01DD                DBYTE BADPRM
                LOC
00CB C4B2               LDI     L(PHEX)-1
00CD 33                 XPAL    P3
00CE C2FF               LD      HI(P2)
00D0 3F                 XPPC    P3
00D1 C2FE               LD      LO(P2)
00D3 02                 CCL                     ;CLEAR CARRY/LINK FLAG
00D4 F4FF               ADI     -1              ;CORRECT COUNT
00D6 3F                 XPPC    P3
00D7 9090               JMP     RETN2
                OK
00D9 02                 CCL
00DA C400               LDI     0
00DC CAE9               ST      DPHI(P2)        ;CLEAR UPPER D.P. COUNT
00DE FAEB               CAD     HCNT(P2)        ;COMPLEMENT HIT COUNT
00E0 CAEB               ST      HCNT(P2)
00E2 02                 CCL                     ;CLEAR CARRY/LINK FLAG
00E3 F2EB               ADD     HCNT(P2)        ;COMPUTE 5X
00E5 CAEA               ST      DPLO(P2)
00E7 C400               LDI     0
00E9 F2E9               ADD     DPHI(P2)
00EB CAE9               ST      DPHI(P2)        ;2X
00ED 02                 CCL
00EE C2EA               LD      DPLO(P2)
00F0 F2EA               ADD     DPLO(P2)
00F2 CAEA               ST      DPLO(P2)
00F4 C2E9               LD      DPHI(P2)
00F6 F2E9               ADD     DPHI(P2)
00F8 CAE9               ST      DPHI(P2)        ;4X
00FA 02                 CCL
00FB C2EB               LD      HCNT(P2)
00FD F2EA               ADD     DPLO(P2)
00FF CAEA               ST      DPLO(P2)
0101 C400               LDI     0
0103 F2E9               ADD     DPHI(P2)
0105 CAE9               ST      DPHI(P2)        ;5X
                PRLP
0107 3D                 XPPC    P1              ;PROGRAM PROM
0108 BAEA               DLD     DPLO(P2)        ;DECREMENT LOWER COUNT
010A 9CFB               JNZ     PRLP            ;NOT DONE
010C BAE9               DLD     DPHI(P2)        ;DECREMENT UPPER COUNT
010E 94F7               JP      PRLP            ;NOT DONE
0110 C2FD               LD      SAVLO(P2)       ;RESTORE P1
0112 31                 XPAL    P1
0113 C2FC               LD      SAVHI(P2)
0115 35                 XPAH    P1
                UPDATE
0116 CB01               ST      CLK(P3)         ;BUMP PROM COUNTER
0118 BAEF               DLD     LO(P2)          ;DECREMENT LOWER LOC COUNT
011A 9C8D               JNZ     NXTLOC          ;NOT DONE
011C BAEF               DLD     HI(P2)          ;DECREMENT UPPER LOC COUNT
011E 9489               JP      NXTLOC          ;NOT DONE
0120 9051               JMP     RETN1           ;PROGRAMMING DONE
                PPROM
0122 C400               LDI     0
0124 CB0C               ST      RD(P3)          ;TURN OFF READ MODE AND
0126 CB1C               ST      CS(P3)          ; CHIP SELECT
0128 40                 LDE
0129 CB00               ST      LOAD(P3)        ;SEND DATA TO PROGRAMMER
012B C401               LDI     1
012D CB04               ST      VSS(P3)         ;TURN ON VSS VOLTAGE
012F C47F               LDI     07F             ;WAIT 500 MICROSECONDS
0131 8F00               DLY     0
0133 CB14               ST      VP(P3)          ;TURN ON PROGRAM PULSE
0135 C4FF               LDI     OFF
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278 0137 8F00           DLY     0               ;DELAY 1 MS
279 0139 C400           LDI     0
280 013B CB14           ST      VP(P3)          ;TURN OFF VP
281 013D C414           LDI     20              ;WAIT 100 MICROSECONDS
282 013F 8F00           DLY     0
283 0141 C400           LDI     0
284 0143 CB04           ST      VSS(P3)         ;TURN OFF VSS VOLTAGE
285 0145 C414           LDI     20              ;WAIT 100 MICROSECONDS
286 0147 8F00           DLY     0
287 0149 CB0C           ST      RD(P3)          ;SET UP READ MODE
288 014B CB1C           ST      CS(P3)          ;SELECT PROM SOCKET
289 014D C400           LDI     0
290 014F CB00           ST      LOAD(P3)        ;CLEAR DATA LATCHES
291 0151 C302           LD      RDPRM(P3)       ;READ DATA FROM PROM
292 0153 3D             XPPC    P1
293 0154 90CC           JMP     PPROM
294
295                 ; COPY PROM TO RANGE IN MEMORY
296
297                 COPY
298 0156 C401           JS      P1,SETRD        ;SET READ MODE
    0158 35C4
    015A A531
    015C 3D
299 015D C601           LD      @1(P2)          ;RETRIEVE ADDR  FROM STACK
300 015F F402           ADI     2               ;ADD 512 OFFSET
301 0161 35             XPAH    P1
302 0162 C601           LD      @1(P2)
303 0164 31             XPAL    P1
304                 CPLOOP
305 0165 C302           LD      RDPRM(P3)       ;GET PROM DATA
306 0167 CDFF           ST      @-1(P1)         ;STORE INTO MEMORY
307 0169 CB01           ST      CLK(P3)         ;BUMP PROM COUNTER
308 016B BAFE           DLD     LO(P2)          ;DECREMENT LOC COUNTER LOW
309 016D 9CF8           JNZ     CPLOOP
310 016F BAFF           DLD     HI(P2)          ;DECREMENT LOC COUNTER HIGH
311 0171 94F2           JP      CPLOOP          ;NOT DONE
312                 RETN1
313 0173 C400           LDI     H(PROMPT)
314 0175 35             XPAH    P1
315 0176 C406           LDI     L(PROMPT)-1
316 0178 31             XPAL    P1
317 0179 3D             XPPC    P1
318
319                 ; VERIFY PROM AGAINST RANGE IN MEMORY
320
321                 VERIFY
322 017A C401           JS      P1,SETRD        ;SET READ MODE
    017C 35C4
    017E A531
    0180 3D
323 0181 C601           LD      @1(P2)
324 0183 F402           ADI     2               ;ADD 512 OFFSET
325 0185 35             XPAH    P1
326 0186 C601           LD      @1(P2)
327 0188 31             XPAL    P1
328                 VLOOP
329 0189 C302           LD      RDPRM(P3)       ;GET DATA FROM PROM
330 018B F5FE           XOR     @-1(P1)         ;COMPARE AGAINST MEM  DATA
331 018D 9C0C           JNZ     NOVFY           ;DOES NOT VERIFY
332 018F CB01           ST      CLK(P3)         ;BUMP PROM COUNTER
333 0191 BAFE           DLD     LO(P2)          ;DECREMENT LOC COUNTER LOW
334 0193 9CF4           JNZ     VLOOP           ;NOT DONE
335 0195 BAFF           DLD     HI(P2)          ;DECREMENT LOC COUNTER HIGH
336 0197 94F0           JP      VLOOP           ;NOT DONE
337 0199 90D8           JMP     RETN1
338                 NOVFY
339 019B C47B           JS      P3,MESG         ;GO TO MESSAGE ROUTINE
    019D 37C4
    019F 1633
    01A1 3F
340 01A2 01D1            DBYTE NVRFY
341 01A4 90CD           JMP     RETN1
342                 SETRD
343 01A6 C47B           JS      P3,GHEX         ;GET ADDR  TO COPY TO
    01A8 37C4
    01AA 4F33
    01AC 3F
344 01AD C480           LDI     H(PPROGMR)      ;PUT ADDR  OF PROGRAMMER
345 01AF 37             XPAH    P3              ;  IN P3
346 01B0 C400           LDI     L(PPROGMR)
347 01B2 33             XPAL    P3
348 01B3 C401           LDI     1               ;SET UPPER LOC COUNTER
349 01B5 CAF1           ST      HI+2(P2)
350 01B7 CB0C           ST      RD(P3)          ;SET READ MODE
351 01B9 CB1C           ST      CS(P3)          ;SELECT PROM SOCKET
352 01BB C400           LDI     0
353 01BD CAF0           ST      LO+2(P2)
354 01BF CB03           ST      CLR(P3)         ;CLEAR PROM COUNTER
355 01C1 CB00           ST      LOAD(P3)        ;CLEAR PROM DATA LATCHES
356 01C3 3D             XPPC    P1
357
358                      PAGE   'MESSAGES AND COMMAND TABLE'
359
360                 ; MESSAGES
361
362                 NOTMSG:
363 01C4 0D0A            DBYTE 0D0A
364 01C6 4E4F            ASCII 'NOT ERASED'
    01C8 5420
    01CA 4552
    01CC 4153
    01CE 4544
365 01D0 00              BYTE  0
366                 NVRFY:
367 01D1 0D0A            DBYTE 0D0A
368 01D3 4E4F            ASCII 'NO VERIFY'
    01D5 2056
    01D7 4552
    01D9 4946
    01DB 59
369 01DC 00              BYTE  0
370                 BADPRM:
371 01DD 0D0A            DBYTE 0D0A
372 01DF 4241            ASCII 'BAD PROM AT '
    01E1 4420
    01E3 5052
    01E5 4F4D
    01E7 2041
    01E9 5420
373 01EB 00              BYTE  0
374                 PRMPT:
375 01EC 0D0A            DBYTE 0D0A
376 01EE 3F              BYTE  '?',0
    01EF 00
377
378                       COMMAND TABLE
379
380                 CMDTBL:
381 01F0 50              BYTE  'P'
382 01F1 0081            DBYTE PROG-1
383 01F3 59              BYTE  'Y'
384 01F4 006A            DBYTE WOCHK-1
385 01F6 45              BYTE  'E'
386 01F7 003A            DBYTE ERASED-1
387 01F9 56              BYTE  'V'
388 01FA 0179            DBYTE VERIFY-1
389 01FC 43              BYTE  'C'
390 01FD 0155            DBYTE COPY-1
391 01FF 00              BYTE  0
392
393       0000           END
```
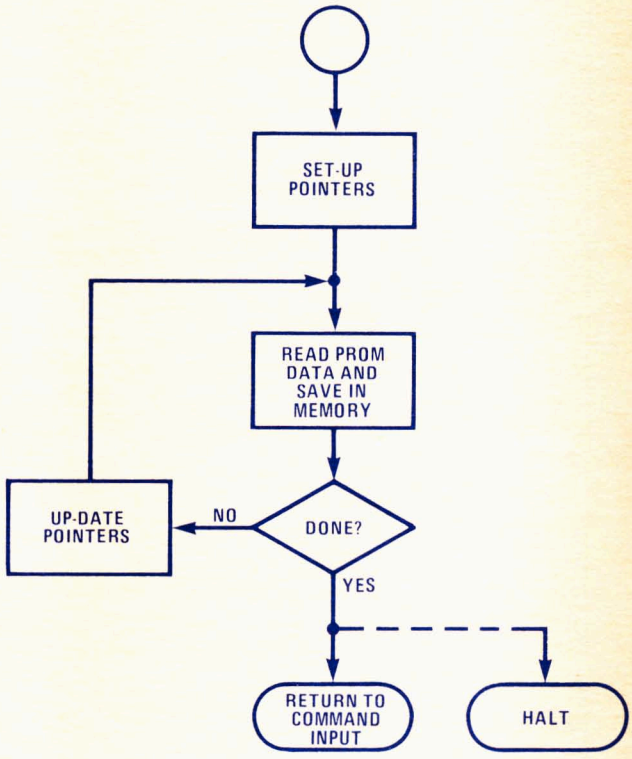

```
BADPRM 01DD     CLK    0001     CLOOP  0021     CLR    0003
CMDTBL 01F0     COPY   0156     CPLOOP 0165     CS     001C
DPHI   FFE9     DPLO   FFEA     ELOOP  0051     ENBL   0004 *
ENTRY  0001 *   ERASED 003B     ERROR  0033     GECHO  7A91
GHEX   7B50     GO     00BA     HCNT   FFEB     HI     FFEF
LO     FFEE     LOAD   0000     LOC    00CB *   MESG   7B17
NOT    0060     NOTMSG 01C4     NOVFY  019B     NPROG  00C2 *
NVRFY  01D1     NXTLOC 00A9     OK     00D9     P1     0001
P2     0002     P3     0003     PHEX   7BB3     PPRGMR 8000
PPROM  0122     PRLP   0107     PRMPT  01EC     PROG   0082
PROMPT 0007     PUTC   7AE2     RD     000C     RDPRM  0002
RETN1  0173     RETN2  0069     SAVHI  FFEC     SAVLO  FFED
SET    009F     SETRD  01A6     STACK  77D0     THSLOC 00AC *
UPDATE 0116 *   VERIFY 017A     VLOOP  0189     VP     0014
VSS    0004     WOCHK  006B

NO ERROR LINES
SOURCE CHECKSUM = 19B0
```

```
1                       TITLE  'PNLPGM:   SC/MP PROM PROGRAMMER'
2
3                   ; "PNLPGM" IS A PROGRAM THAT ALLOWS THE SC/MP LCDS
4                   ; TO PROGRAM MM5204 OR MM4204 PROMS USING THE
5                   ; PANEL FOR ALL INPUTS FROM THE USER
6                   ;
7                   ; THE USER MUST ENTER THE STARTING HEX ADDRESS TO
8                   ; BE PROGRAMMED FROM OR COPIED TO INTO POINTER #1
9                   ; BEFORE EXECUTING EACH ROUTINE
10                  ;
11                  ; THE PROGRAM REQUIRES THAT THERE ARE 512
12                  ; CONTINUOUS MEMORY LOCATIONS UPWARDS FROM THE
13                  ; CONTENTS OF POINTER #1
14                  ;
15                  ; "PNLPGM" USES MEMORY ON THE LCDS MOTHERBOARD FOR
16                  ; TEMPORARY STORAGE.  THEREFORE, USER R/W MEMORY
17                  ; CAN BE ANYWHERE, EXCEPT AS SHOWN BELOW
18                  ;
19                  ; "PNLPGM" CAN BE ASSEMBLED ANYWHERE THE USER HAS
20                  ; MEMORY SPACE EXCEPT IN THE FOLLOWING LOCATIONS:
21                  ;
22                  ;   X'8000 -- X'83FF       LOCATIONS OCCUPIED BY
23                  ;                          PROGRAMMER HARDWARE
24                  ;   X'7000 -- X'7FFF       LOCATIONS USED BY LCDS
25                  ;
26                  ; THE ENTRY POINTS ARE:
27                  ;
28                  ;   NAME      ADDRESS
29                  ;   ----      -------
30                  ;
31                  ; CKERSD      X'0001     CHECK PROM FOR ERASED
32                  ; WOCHK       X'0035     PROGRAM PROM WITHOUT CHECK
33                  ;                        FOR ERASED
34                  ; PROG        X'0048     PROGRAM PROM WITH CHECK FOR
35                  ;                        ERASED
36                  ; COPY        X'0101     COPY PROM INTO MEMORY
37                  ; VERIFY      X'012C     VERIFY PROM AGAINST MEMORY
38                  ;
39                  ; "PNLPGM" HALTS WHEN FINISHED OR ON ERRORS.  THE
40                  ; ERROR HALTS ARE:
41                  ;
42                  ;   X'0035   PROM NOT ERASED
43                  ;   X'0085   PROM CANNOT BE PROGRAMMED
44                  ;   X'015A   PROM DOES NOT VERIFY
45                  ;
46                  ; THE "HALT INST" SWITCH ON THE LCDS MOTHERBOARD
47                  ; MUST BE IN THE "DEBUG" POSITION BEFORE EXECUTION.
48                  ;
49                        PAGE   'POINTERS AND CONSTANTS'
50                  ;
51 0000                  =0
52                  ;
53       0001   P1      =     1
54       0002   P2      =     2
55       0003   P3      =     3
56                  ;
57       8000   PPRGMR  =     08000   ;PERIPHERAL ADDR  OF PROM
58                                     ; PROGRAMMER BOARD
59       0014   VP      =     014     ;ORDER CODE FOR PROG  VOLTAGE
60       000C   RD      =     0C      ;ORDER CODE FOR READ
61       0004   VSS     =     04      ;ORDER CODE FOR VSS,VBB,VDD
62       001C   CS      =     01C     ;ORDER CODE FOR CHIP SELECT
63       0000   LOAD    =     0       ;ORDER CODE TO LOAD DATA
64       0001   CLK     =     1       ;ORDER CODE TO CLOCK COUNTER
65       0002   RDPRM   =     2       ;ORDER CODE TO READ FROM
66                                     ; DATA
67       0003   CLR     =     3       ;ORDER CODE TO CLEAR COUNTER
68       0004   ENBL    =     4       ;ORDER CODE TO ENABLE CONTROL
69                                     ; LATCH
70       77D0   RAM     =     077D0   ;RAM POINTER TO MOTHERBOARD
71                                     ; R/W MEMORY
72       0000   HI      =     0       ;TEMPORARY LOCATIONS IN RAM
73       FFFF   LO      =     -1
```

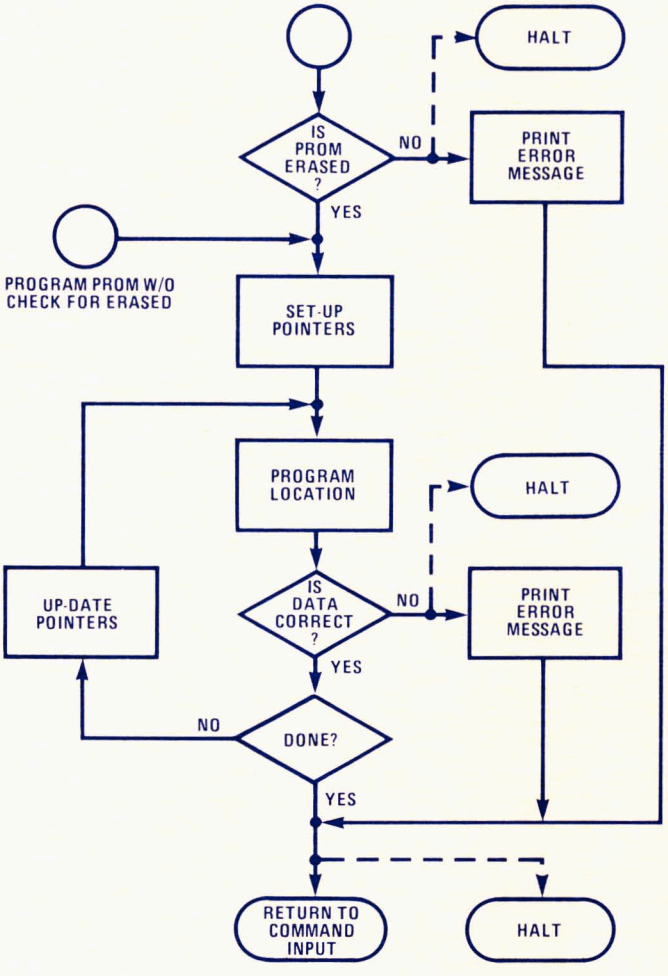
```
                FFFF  SAVLO   =     -2
                FFFE  SAVHI   =     -3
                FFFD  HCNT    =     -4
                FFFC  DPLO    =     -5
                FFFB  DPHI    =     -6

                                PAGE    'PROM ACCESS AND PROGRAMMING ROUTINES'

                        ROUTINE TO CHECK PROM FOR ERASED CONDITION

0000 08                         NOP
                CHERSD
0001 C408                       LDI   L(ERASED)-1
0003 31                         XPAL  P1
0004 C400                       LDI   H(ERASED)
0006 35                         XPAH  P1
0007 3D                         XPPC  P1
0008 00                         HALT                  ;HALT IF ERASED

                        THIS SUBROUTINE IS ALSO CALLED BY "PROG " TO
                        VERIFY THAT THE PROM IS ERASED

                ERASED
0009 C4D0                       LDI   L(RAM)          ;INIT RAM POINTER
000B 32                         XPAL  P2
000C C477                       LDI   H(RAM)
000E 36                         XPAH  P2
                ERAS2
000F C480                       LDI   H(PPRGMR)  ;SET ADDR  OF PROGRAMMER
0011 37                         XPAH  P3
0012 C400                       LDI   L(PPRGMR)
0014 33                         XPAL  P3
0015 C401                       LDI   1               ;SET UPPER COUNT
0017 CA00                       ST    HI(P2)          ;STACK IS EMPTY, USE AS PTR
0019 CB0C                       ST    RD(P3)          ;SET READ MODE
001B CB1C                       ST    CS(P3)          ;SELECT PROM SOCKET
001D C400                       LDI   0               ;SET LOWER COUNT
001F CAFF                       ST    LO(P2)
0021 CB03                       ST    CLR(P3)         ;CLEAR PROM COUNTER
0023 CB00                       ST    LOAD(P3)        ;CLEAR DATA LATCHES FOR READ
                ELOOP
0025 C302                       LD    RDPRM(P3)       ;READ DATA OUT OF PROM
0027 9C0B                       JNZ   NOT             ;DATA NOT ZERO? NOT ERASED
0029 CB01                       ST    CLK(P3)         ;DATA OK, BUMP COUNTER
002B BAFF                       DLD   LO(P2)          ;DECREMENT LOWER COUNT
002D 9CFA                       JNZ   ELOOP           ;NOT DONE YET
002F BA00                       DLD   HI(P2)          ;DECREMENT UPPER COUNT
0031 94F2                       JP    ELOOP           ;NOT DONE YET
0033 3D                         XPPC  P1              ;PROM IS ERASED
                NOT
0034 00                         HALT                  ;HALT IF PROM NOT ERASED

                        ENTRY POINT TO PROGRAM PROM W/O CHECK FOR ERASED

                WOCHK
0035 02                         CCL
0036 C477                       LDI   H(RAM)          ;INIT RAM POINTER
0038 36                         XPAH  P2
0039 C4D0                       LDI   L(RAM)
003B 32                         XPAL  P2
003C C480                       LDI   H(PPRGMR)
003E 37                         XPAH  P3
003F C400                       LDI   L(PPRGMR)
0041 33                         XPAL  P3
0042 35                         XPAH  P1
0043 F402                       ADI   2               ;ADD 512 OFFSET
0045 35                         XPAH  P1
0046 9019                       JMP   SET

                ; ENTRY POINT TO PROGRAM PROM W/CHECK FOR ERASED

                ; PROM IS PROGRAMMED FROM MOST SIGNIFICANT ADDRESS
                ; TO LEAST SIGNIFICANT ADDRESS DUE TO INVERSION OF
                ; COUNTER

                PROG
0048 02                         CCL
0049 C4D0                       LDI   L(RAM)
004B 32                         XPAL  P2
004C C477                       LDI   H(RAM)
004E 36                         XPAH  P2
004F 31                         XPAL  P1              ;SAVE ADDRESS
0050 CAFE                       ST    SAVLO(P2)
0052 35                         XPAH  P1
0053 CAFD                       ST    SAVHI(P2)
0055 C40F                       LDI   L(ERAS2)-1 ;CHECK PROM FOR ERASED
0057 31                         XPAL  P1
0058 3D                         XPPC  P1
0059 C2FE                       LD    SAVLO(P2)
005B 31                         XPAL  P1
005C C2FD                       LD    SAVHI(P2)
005E F402                       ADI   2               ;ADD 512 OFFSET
0060 35                         XPAH  P1
0061 C401               SET     LDI   1
0063 CA00                       ST    HI(P2)          ;SET UPPER LOC COUNT
0065 C400                       LDI   0
0067 CAFF                       ST    LO(P2)          ;SET LOWER LOC COUNT
0069 CB03                       ST    CLR(P3)         ;CLEAR PROM COUNTER
                NXTLOC
006B C5FF                       LD    @-1(P1)         ;GET DATA TO PROGRAM
006D 01                         XAE                   ;SAVE IN EXTENSION REG
                THSLOC
006E C400                       LDI   H(PPROM)   ;SET ADDR  OF PROGRAMMING RTN
0070 35                         XPAH  P1
0071 CAFD                       ST    SAVHI(P2)  ;SAVE PTR ADDR
0073 C4CC                       LDI   L(PPROM)-1
0075 31                         XPAL  P1
0076 CAFE                       ST    SAVLO(P2)
0078 C4FE                       LDI   -2              ;SET COUNT
007A CAFC                       ST    HCNT(P2)  ;SAVE HIT COUNT IN RAM
                GO
007C 3D                         XPPC  P1
007D 60                         XRE                   ;CHECK PROM DATA
007E 9805                       JZ    OK              ;PROM DATA CORRECT, DO X+5X
0080 BAFC                       DLD   HCNT(P2)  ;DECREMENT HIT COUNT
0082 9CF8                       JNZ   GO              ;CHECK FOR MAX  HIT
                NPROG
0084 00                         HALT                  ;HIT COUNT OVER MAX, BAD PROM
                OK
0085 02                         CCL
0086 C400                       LDI   0
0088 CAFA                       ST    DPHI(P2)  ;CLEAR UPPER D.P.  COUNT
008A FAFC                       CAD   HCNT(P2)  ;COMPLEMENT HIT COUNT
008C CAFC                       ST    HCNT(P2)
008E 02                         CCL                   ;CLEAR CARRY/LINK FLAG
008F F2FC                       ADD   HCNT(P2)  ;COMPUTE 5X
0091 CAFB                       ST    DPLO(P2)
0093 C400                       LDI   0
0095 F2FA                       ADD   DPHI(P2)
0097 CAFA                       ST    DPHI(P2)  ;2X
0099 02                         CCL
009A C2FB                       LD    DPLO(P2)
009C F2FB                       ADD   DPLO(P2)
009E CAFB                       ST    DPLO(P2)
00A0 C2FA                       LD    DPHI(P2)
00A2 F2FA                       ADD   DPHI(P2)
00A4 CAFA                       ST    DPHI(P2)  ;4X
00A6 02                         CCL
00A7 C2FC                       LD    HCNT(P2)
00A9 F2FB                       ADD   DPLO(P2)
00AB CAFB                       ST    DPLO(P2)
00AD C400                       LDI   0
00AF F2FA                       ADD   DPHI(P2)
00B1 CAFA                       ST    DPHI(P2)  ;5X
                PRLP
00B3 3D                         XPPC  P1              ;PROGRAM PROM
00B4 BAFB                       DLD   DPLO(P2)  ;DECREMENT LOWER COUNT
00B6 9CFB                       JNZ   PRLP            ;NOT DONE
00B8 BAFA                       DLD   DPHI(P2)  ;DECREMENT UPPER COUNT
00BA 94F7                       JP    PRLP            ;NOT DONE
00BC C2FE                       LD    SAVLO(P2) ;RESTORE P1
00BE 31                         XPAL  P1
00BF C2FD                       LD    SAVHI(P2)
00C1 35                         XPAH  P1
                UPDATE
00C2 CB01                       ST    CLK(P3)         ;BUMP PROM COUNTER
00C4 BAFF                       DLD   LO(P2)          ;DECREMENT LOWER LOC COUNT
00C6 9CA3                       JNZ   NXTLOC          ;NOT DONE
00C8 BA00                       DLD   HI(P2)          ;DECREMENT UPPER LOC COUNT
00CA 949F                       JP    NXTLOC          ;NOT DONE
00CC 00                         HALT                  ;HALT WHEN DONE
                PPROM
00CD C400                       LDI   0
00CF CB0C                       ST    RD(P3)          ;TURN OFF READ MODE AND
00D1 CB1C                       ST    CS(P3)          ;  CHIP SELECT
00D3 40                         LDE
00D4 CB00                       ST    LOAD(P3)        ;SEND DATA TO PROGRAMMER
00D6 C401                       LDI   1
00D8 CB04                       ST    VSS(P3)         ;TURN ON VSS VOLTAGE
00DA C47F                       LDI   07F             ;WAIT 500 MICROSECONDS
00DC 8F00                       DLY   0
00DE CB14                       ST    VP(P3)          ;TURN ON PROGRAM PULSE
00E0 C4FF                       LDI   0FF
00E2 8F00                       DLY   0               ;DELAY 1 MS
00E4 C400                       LDI   0
00E6 CB14                       ST    VP(P3)          ;TURN OFF VP
00E8 C414                       LDI   20              ;WAIT 100 MICROSECONDS
00EA 8F00                       DLY   0
00EC C400                       LDI   0
00EE CB04                       ST    VSS(P3)         ;TURN OFF VSS VOLTAGE
00F0 C414                       LDI   20              ;WAIT 100 MICROSECONDS
00F2 8F00                       DLY   0
00F4 CB0C                       ST    RD(P3)          ;SET UP READ MODE
00F6 CB1C                       ST    CS(P3)          ;SELECT PROM SOCKET
00F8 C400                       LDI   0
00FA CB00                       ST    LOAD(P3)        ;CLEAR DATA LATCHES
00FC C302                       LD    RDPRM(P3)  ;READ DATA FROM PROM
00FE 3D                         XPPC  P1
00FF 90CC                       JMP   PPROM

                ; COPY PROM TO RANGE IN MEMORY

                COPY
0101 02                         CCL
0102 C477                       LDI   H(RAM)
0104 36                         XPAH  P2
0105 C4D0                       LDI   L(RAM)
0107 32                         XPAL  P2              ;INIT RAM POINTER
0108 31                         XPAL  P1
0109 CAFE                       ST    SAVLO(P2)
010B 35                         XPAH  P1
010C F402                       ADI   2               ;ADD 512 OFFSET
010E CAFD                       ST    SAVHI(P2)
0110 C401                       JS    P1,SETRD        ;SET READ MODE
0112 35C4
0114 5931
0116 3D
0117 C2FD                       LD    SAVHI(P2)  ;RETRIEVE ADDRESS
0119 35                         XPAH  P1
011A C2FE                       LD    SAVLO(P2)
011C 31                         XPAL  P1
                CPLOOP
011D C302                       LD    RDPRM(P3)  ;GET PROM DATA
011F CDFF                       ST    @-1(P1)         ;STORE INTO MEMORY
0121 CB01                       ST    CLK(P3)         ;BUMP PROM COUNTER
0123 BAFF                       DLD   LO(P2)          ;DECREMENT LOC COUNTER LOW
0125 9CF6                       JNZ   CPLOOP
0127 BA00                       DLD   HI(P2)          ;DECREMENT LOC COUNTER HIGH
0129 94F2                       JP    CPLOOP          ;NOT DONE
012B 00                         HALT                  ;HALT WHEN DONE

                        VERIFY PROM AGAINST RANGE IN MEMORY

                VERIFY
012C 02                         CCL
012D C477                       LDI   H(RAM)
012F 36                         XPAH  P2
0130 C4D0                       LDI   L(RAM)
0132 32                         XPAL  P2              ;INIT RAM POINTER
0133 31                         XPAL  P1
0134 CAFE                       ST    SAVLO(P2)
0136 35                         XPAH  P1
0137 F402                       ADI   2               ;ADD 512 OFFSET
0139 CAFD                       ST    SAVHI(P2)
013B C401                       JS    P1,SETRD        ;SET READ MODE
013D 35C4
013F 5931
0141 3D
```

```
306 0142 C2FD            LD    SAVHI(P2)   ;RETRIEVE ADDRESS
307 0144 35              XPAH  P1
308 0145 C2FE            LD    SAVLO(P2)
309 0147 31              XPAL  P1
310              VLOOP
311 0148 C302            LD    RDPRM(P3)   ;GET DATA FROM PROM
312 014A E5FF            XOR   @-1(P1)     ;COMPARE AGAINST MEMORY DATA
313 014C 9C0B            JNZ   NOVFY       ;DOES NOT VERIFY
314 014E CB01            ST    CLK(P3)     ;BUMP PROM COUNTER
315 0150 BAFF            DLD   LO(P2)      ;DECREMENT LOC COUNTER LOW
316 0152 9CF4            JNZ   VLOOP       ;NOT DONE
317 0154 BA00            DLD   HI(P2)      ;DECREMENT LOC COUNTER HIGH
318 0156 94F0            JP    VLOOP       ;NOT DONE
319 0158 00              HALT              ;HALT WHEN DONE
320              NOVFY
321 0159 00              HALT              ;HALT ON ERROR
322              SETRD
323 015A C480            LDI   H(PPRGMR)   ;PUT ADDR. OF PROGRAMMER
324 015C 37              XPAH  P3          ;  IN P3
325 015D C400            LDI   L(PPRGMR)
326 015F 33              XPAL  P3
327 0160 C401            LDI   1           ;SET UPPER LOC COUNTER
328 0162 CA00            ST    HI(P2)
329 0164 CB0E            ST    RD(P3)      ;SET READ MODE
330 0166 CB1C            ST    CS(P3)      ;SELECT PROM SOCKET
331 0168 C400            LDI   0
332 016A CAFF            ST    LO(P2)
333 016C CB03            ST    CLR(P3)     ;CLEAR PROM COUNTER
334 016F CB00            ST    LOAD(P3)    ;CLEAR PROM DATA LATCHES
335 0170 3D              XPPC  P1
336      0000             END

CKERSD 0001 *   CLK     0001     CLR     0003     COPY    0101 *
CPLOOP 011D     CS      001C     DPHI    FFFA     DPLO    FFFB
ELOOP  0025     ENBL    0004 *   ERAS2   000F     ERASED  0009
GO     007C     HCNT    FFFC     HI      0000     LO      FFFF
LOAD   0000     NOT     0034     NOVFY   0159     NPROG   0084 *
NXTLOC 006B     OK      0085     P1      0001     P2      0002
P3     0003     PPRGMR  8000     PPROM   00CD     PRLP    00B3
PROG   0048 *   RAM     7700     RD      000C     RDPRM   0002
SAVHI  FFFD     SAVLO   FFFE     SET     0061     SETRD   015A
THSLOC 006F *   UPDATE  00C2 *   VERIFY  012C *   VLOOP   0148
VP     0014     VSS     0004     WOCHK   0035 *

NO ERROR LINES
SOURCE CHECKSUM = C17D
```

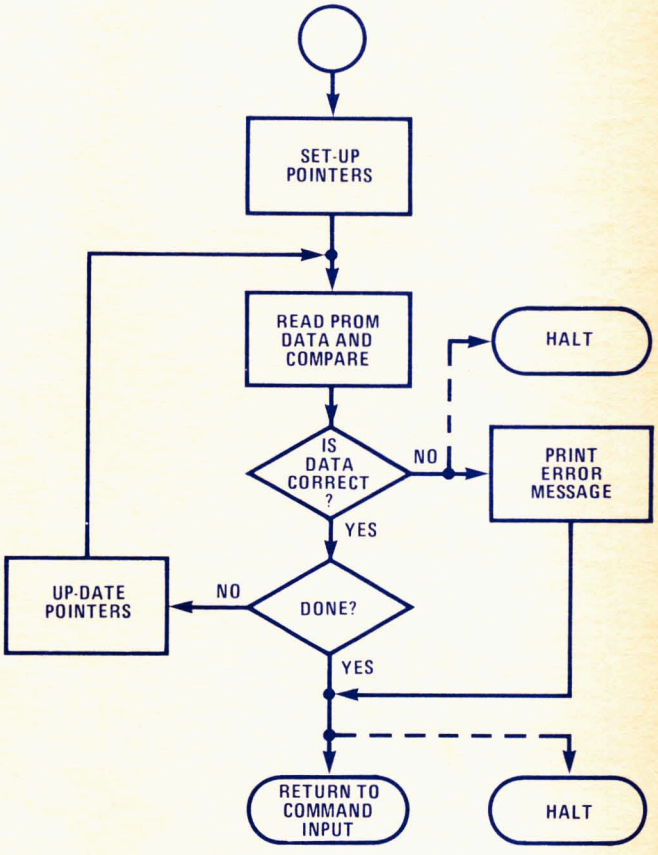
COPY PROM INTO MEMORY



PROGRAM PROM W/CHECK FOR ERASED



VERIFY PROM AGAINST MEMORY



NOTE: DASHED LINES INDICATE PANEL PROGRAM ERRORS & EXITS.

New Library Programs

PACE BASIC PROGRAM
SL0048A BIORHYTHM

Source paper tapes $5.00 each

This program plots the three biorhythm curves (physical, emotional, and intellectual) for any time period after the given birthdate.

```
1 DIM T(12)
2 N$="000102030405060708091011121314151617181920212223242526"
3 N$=N$+"2728293031"
4 REM BIORHYTHM CREATED BY JOY AND RICHARD FOX
6 PRINT "DO YOU WISH AN INTRODUCTION TO BIORHYTHM?"
8 INPUT "YES OR NO";A$
9 IF A$="NO" THEN 27
10 PRINT
11 PRINT TAB(25);"BIORHYTHM"
12 PRINT
13 PRINT
15 PRINT " THE PURPOSE OF BIORHYTHM IS TO PREDICT A PHYSICAL,"
16 PRINT "EMOTIONAL AND INTELLECTUAL PATTERN THAT INDICATES YOUR"
17 PRINT "UP AND DOWN DAYS FOR ANY PERIOD OF TIME. BIORHYTHM CAN"
18 PRINT "SHOW WHICH DAYS WERE GOOD OR BAD FOR YOU BEGINNING WITH"
19 PRINT "YOUR BIRTH. IT CAN ALSO SHOW YOU WHICH OF YOUR FUTURE"
20 PRINT "DAYS WILL BE GOOD OR BAD FOR YOU."
21 PRINT " THESE PREDICTIONS ARE BASED ON SCIENTIFIC STUDIES TO"
22 PRINT "DETERMINE WHY ACCIDENTS OCCUR. IT WAS LEARNED THROUGH"
23 PRINT "THESE STUDIES THAT A PHYSICAL CYCLE OCCURS EVERY 23 DAYS,"
24 PRINT "AN EMOTIONAL CYCLE EVERY 28 DAYS, AND AN INTELLECTUAL"
25 PRINT "CYCLE EVERY 33 DAYS."
26 PRINT
27 PRINT "PLEASE TYPE YOUR BIRTH DATE USING THE FOLLOWING FORMAT"
28 PRINT "MM,DD,YY. EXAMPLE: JANUARY 17, 1942 = 01,17,42"
40 INPUT M,D,Y
45 PRINT "AT WHAT DATE ARE YOU INTERESTED IN BEGINNING BIORHYTHM?"
46 PRINT "(THE YEAR MUST BE GREATER THAN YOUR BIRTH YEAR)"
50 INPUT M1,D1,Y1
55 IF Y1 <= Y THEN 45
60 PRINT "HOW MANY DAYS DO YOU WISH TO HAVE PLOTTED?"
65 INPUT D2
80 DATA 31,28,31,30,31,30,31,31,30,31,30,31
110 REM M=MONTH,D=DAY,Y=YEAR
120 REM D3=TOTAL NUMBER OF DAYS ELAPSED
130 D3=0
140 IF M>2 THEN 200
150 IF INT(Y/4)-(Y/4)<>0 THEN 200
160 D3=1
190 REM T=DAYS IN EACH MONTH
200 FOR I=1 TO 12
210 READ T(I)
230 NEXT I
240 D3=T(M)-D+D3
250 FOR I=M+1 TO 12
260 D3=T(I)+D3
270 NEXT I
```

```
280 REM Y3=YEAR COUNTER FROM BIRTH TO DISPLAY
290 Y3=Y
299 Y3=Y3+1
305 IF Y3>=Y1 THEN 400
310 IF INT(Y3/4)-(Y3/4)=0 THEN 370
315 D3=D3+365
316 GOTO 299
370 D3=D3+366
325 GOTO 299
400 IF M1<=2 THEN 450
405 IF INT(Y1/4)-(Y1/4)<>0 THEN 450
410 D3=D3+1
450 FOR I=1 TO M1-1
455 D3=T(I)+D3
460 NEXT I
470 D3=D1+D3
475 PRINT "PHYSICAL CYCLE = P"
480 PRINT "EMOTIONAL CYCLE = E"
490 PRINT "INTELLECTUAL CYCLE = I"
491 PRINT
492 PRINT
493 PRINT
500 PRINT "DATE";
505 PRINT TAB(13);"DOWN";
510 PRINT TAB(35);"CRITICAL";
520 PRINT TAB(62);"UP"
525 PRINT "---------";TAB(13);
526 PRINT "-----------------------------------------------------------------"
530 LET M4=M1
540 LET D4=D1
550 LET Y4=Y1
560 REM M4,D4,Y4 = DATE PRINTED OUT IN PLOTTING CHART
570 GOTO 580
571 REM F=FRACTION INTO CYCLE
580 F=(D3/23)-INT(D3/23)
600 REM X=THE ARGUMENT FOR THE SINE FUNCTION
610 X=F*2*3.1416
640 REM P=THE PHYSICAL POSITION ON THE GRAPH
650 P=INT((SIN(X)+1)*25+0.5)
655 REM E=EMOTIONAL POSITION ON THE GRAPH
660 F=(D3/28)-INT(D3/28)
670 X=F*2*3.1416
680 E=INT((SIN(X)+1)*25+0.5)
690 REM I=INTELLECTUAL POSITION ON THE GRAPH
700 F=(D3/33)-INT(D3/33)
710 X=F*2*3.1416
720 I=INT((SIN(X)+1)*25+0.5)
721 REM PRINT THE DATE
722 Y4=Y4 MOD 100
723 PRINT MID$(N$,M4*2+1,2);"/";
724 PRINT MID$(N$,D4*2+1,2);"/";
725 PRINT MID$(N$,INT(Y4/10)*2+2,1);
726 PRINT MID$(N$,(Y4-INT(Y4/10)*10)*2+2,1);TAB(13);
730 A$="  "
732 A$=A$+" "
736 A$=LEFT$(A$,E)+"E"+MID$(A$,E+2)
738 A$=LEFT$(A$,P)+"P"+MID$(A$,P+2)
740 A$=LEFT$(A$,I)+"I"+MID$(A$,I+2)
742 IF I=P THEN A$=LEFT$(A$,I)+"*"+MID$(A$,I+2)
```

```
 744 IF I=E THEN A$=LEFT$(A$,I)+"*"+MID$(A$,I+2)
 746 IF P=E THEN A$=LEFT$(A$,E)+"*"+MID$(A$,E+2)
 747 PRINT A$
 748 IF D2=1 THEN 999
 750 D2=D2-1
 800 D3=D3+1
 810 D4=D4+1
 815 IF M4<>2 THEN 820
 816 IF D4<>29 THEN 820
 817 IF INT(Y4/4)-(Y4/4)<>0 THEN 820
 818 GOTO 570
 820 IF D4<=T(M4) THEN 570
 830 M4=M4+1
 835 D4=1
 840 IF M4>12 THEN 870
 850 GOTO 570
 870 M4=1
 880 Y4=Y4+1
 900 GOTO 570
 999 GETC=$7E3B
1010 CALL GETC ' WAIT FOR RESPONSE BEFORE NEXT
1020 RESTORE
1030 PRINT LIN(4);
1040 INPUT "AGAIN";A$
1050 IF A$<>"NO" THEN 1
1060 END
```

SC/MP ASSEMBLY PROGRAM SL0049A REFLEX

Source paper tape $5.00 each

Program listing see pages 11 and 12

REFLEX is a reflex test program that runs on the SC/MP LCDS. It can be on a PROM in the LCDS PROM socket, or it can be entered into RAM by hand. The program uses the LED's on the LCDS. A dash appears at the left side of the LED's and shifts right, across the LED's. When the dash disappears, the player hits any key on the keyboard. The reflex time is then displayed on the LED's. If you hit a key before the dash disappears, the LED's will display the message ERROR.

To start the program, hit INIT, then hit RUN.

Contributed by: Chuck Bennett
CB Systems
16126 Larch Way
Lynnwood, WA 98036
(206) 624-5998

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IMP-16 ASSEMBLY PROGRAM SL0050A PRTMOD

Source paper tapes $5.00 each

Program listing, see page 12

This program modifies the "HP" command in the IMP-16 Editor program for automatic form feeds with a high speed printer. This overlay patch provides a form feed to the printer after every 60 lines, and two form feeds at the end of the printout. These modifications prevent the printer from printing across page boundaries and ejects the paper for easy removal after the printing is completed.

The patch can be loaded into memory or onto the disc with the disc loader. The overlay cannot be done with the disc loader as it creates too many output sectors on the disc and will overwrite the next program.

Contributed by:

Craig J. Bradley — ARGO Systems
1069 E. Meadow Dr., Palo Alto, CA 94303
(415) 494-6600

```
1                       ;SC/MP ASSEMBLY PROGRAM
2                       ;SL0049A  REFLEX
3                        TITLE SCMP: REFLEX TEST
4 0000                    =     0
5       0000    CNTR1     =     00
6       0001    CNTR2     =     01
7       0002    CNTR3     =     02
8       0003    CNTR4     =     03
9       0004    DIG4      =     04
10      0005    DIG3      =     05
11      0006    DIG2      =     06
12      0007    DIG1      =     07
13      0008    DIG0      =     08
14      0009    DIGA      =     09
15      0080    COUNT1    =     080
16      0010    COUNT2    =     010
17
18 0001 C470    START     LDI   070       ;SET P1
19 0003 35                XPAH  1
20 0004 C477              LDI   077       ;SET P2
```

```
                XPAH  2
0007 C47A       LDI   07A       ;SET P3
                XPAH  3
000A C46F       LDI   06F
000C 33         XPAL  3
000D C400       LDI   0
000F CA02       ST    CNTR3(2)
0011 CA03       ST    CNTR4(2)
0013 CA08       ST    DIG0(2)
0015 CA09       ST    DIGA(2)
0017 C420       LDI   020       ;SET FIRST DASH
0019 01   DASH  XAE
001A C410       LDI   COUNT2    ;SET CNTR 2
001C CA01       ST    CNTR2(2)
001E C480 LOOP2 LDI   COUNT1    ;SET CNTR 1
0020 CA00       ST    CNTR1(2)
0022 C440       LDI   040       ;FIRST DASH
0024 C980       ST    -128(1)
0026 C11F LOOP  LD    01F(1)    ;GET KYBD
0028 D40F       ANI   0F
002A 9C5D       JNZ   ERROR
002C BA00       DLD   CNTR1(2)  ;DEC CNTR 1
002E 9CFA       JNZ   LOOP
0030 BA01       DLD   CNTR2(2)  ;DEC CNTR 2
0032 9CEA       JNZ   LOOP2
0034 01         XAE             ;NEXT DASH
0035 1C         SR
0036 9CF1       JNZ   DASH
0038 C900       ST    (1)       ;BLANK DISPLY
003A 03   COUNT SCL             ;DEC INC CNTR 3
003B C4AA       LDI   170       ;DELAY
003D 8F00       DLY   0
003F C202       LD    CNTR3(2)
0041 FC00       DAI   0
0043 CA02       ST    CNTR3(2)
0045 C203       LD    CNTR4(2)
0047 FC00       DAI   0
0049 CA03       ST    CNTR4(2)
004B C11F       LD    01F(1)    ;GET KYBD
004D D40F       ANI   0F        ;MASK 4 MSB
004F 98E9       JZ    COUNT
0051 C203 CONVERT LD  CNTR4(2)  ;GET MSD
0053 1C         SR
0054 1C         SR
0055 1C         SR
0056 1C         SR
0057 01         XAE
0058 C380       LD    -128(3)
005A CA04       ST    DIG4(2)
005C C203       LD    CNTR4(2)  ;GET MSD -1
005E D40F       ANI   0F
0060 01         XAE
0061 C380       LD    -128(3)
0063 CA05       ST    DIG3(2)
0065 C202       LD    CNTR3(2)  ;GET LSD +1
0067 1C         SR
0068 1C         SR
0069 1C         SR
006A 1C         SR
006B 01         XAE
006C C380       LD    -128(3)
006E CA06       ST    DIG2(2)
0070 C202       LD    CNTR3(2)  ;GET LSD
0072 D40F       ANI   0F
0074 01         XAE
0075 C380       LD    -128(3)
0077 CA07       ST    DIG1(2)
0079 C404 DISPLY LDI  04        ;SET P2 TO DIG 4
007B 32         XPAL  2
007C C420       LDI   020       ;SET TO LEFT DIGIT
007E 01   LOOP1 XAE
007F C601       LD    @1(2)
0081 C980       ST    -128(1)
0083 01         XAE
0084 1C         SR
0085 9CE7       JNZ   LOOP1
0087 90F0       JMP   DISPLY
0089 C479 ERROR LDI   079       ;SET ERROR MSG
008B CA04       ST    DIG4(2)
008D C450       LDI   050
008F CA05       ST    DIG3(2)
0091 CA06       ST    DIG2(2)
0093 CA08       ST    DIG0(2)
0095 C45C       LDI   05C
0097 CA07       ST    DIG1(2)
0099 C400       LDI   0
009B CA09       ST    DIGA(2)
009D 90DA       JMP   DISPLY
      0000       END
```

```
CNTR1  0000   CNTR2  0001   CNTR3  0002   CNTR4  0003
CONVER 0051 *  COUNT  003A   COUNT1 0080   COUNT2 0010
DASH   0019    DIG0   0008   DIG1   0007   DIG2   0006
DIG3   0005    DIG4   0004   DIGA   0009   DISPLY 0079
ERROR  0089    LOOP   0026   LOOP1  007E   LOOP2  001E
START  0001 *

NO ERROR LINES
SOURCE CHECKSUM = A828
```

```
                ;IMP-16 ASSEMBLY PROGRAM
                ;SL0050A  PRTMOD
                 TITLE PRTMOD
0000             .ASECT
                ;
                ; HIGH SPEED PRINTER FORM FEED MODIFICATION
                ;
                ; THIS PROGRAM IS AN OVERLAY PATCH FOR
                ; THE IMP-16 EDITOR (EDIT16 REV E 12/17/75)
                ; IF OTHER REVISION LEVEL EDITORS ARE USED
                ; IT WILL BE NECESSARY TO CHANGE THE ASSEMBLER
                ; ADDRESS DIRECTIVES TO RELOCATE THE PATCHES
                ; AND REDEFINE THE BASE PAGE DEFINITIONS
                ;
```

```
                ; PROGRAMER:             CRAIG J. BRADLEY
                ;                        ARGOSYSTEMS INC
                ;                        1977
                ;
                ; TO MODIFY THE PROGRAM
                ; 1  LOAD THE EDITOR FROM PAPER TAPE
                ;    (DO NOT LOAD FROM DISC AS THIS WILL START
                ;    THE PROGRAM AND CHANGE THE CODE)
                ; 2  LOAD THIS PROGRAM FROM PAPER TAPE
                ; 3  PUNCH A LM PAPER TAPE USING RAMDUMP FROM
                ;    LOCATION 0000 TO 0D6F
                ; 4  USING DSCLDR WRITE THE PROGRAM TO OSC ON
                ;    THE DISC
                ;         DSCLDR COMMANDS
                ;         'CLR
                ;         'MP 05C
                ;         'OBS 0
                ;         'DTS 0
                ;         'RLM        ;DSCLDR READS PT
                ;         'GO 0CF0    ;START ADDR OF EDIT16
                ;         DSCLDR WILL  WRITE TO DISC. PRINT
                ;         ADDRESS RANGES AND DISC SECTORS
                ;         (005C 0069)
                ;
                ; NOTE:   IF DSCLDR IS USED TO DO THE OVERLAY
                ;         TOO MANY DISC SECTORS WILL BE USED AND
                ;         THE PROGRAM WILL OVER-WRITE THE NEXT
                ;         PROGRAM ON THE DISC
                 PAGE
                ; DEFINITIONS
                ;
003C A MAXCNT  =60              ;MAX LINES / PAGE
                ;
                ; BASE PAGE DEFINITIONS
                ;
0014 A DEVICE  =0014
004C A H0A     =004C
0072 A SPUTC   =0072
                ;
                ; TOP SECTOR DEFINITIONS
                ;
0765 A HSPRT   =0765
0005 A  SPACE 5
0000            =0079
                ;
                ; CHANGE 'TYPE' POINTER TO 'MESG' IN PROM
                ;
0079 7EC3 A STYPE    WORD   07EC3
007A            =007F
                ;
                ; CHANGE PRINTER ROUTINE POINTER
                ;
007F 07A9 A ADHSP    WORD   HSPRT1
0080            =02A9
                ;
                ; NO-OP CARD READER COMMAND
                ;
02A9 0000 A          WORD   0
02AA            =069F
                ;
                ; REPLACES INSTRUCTION     LI  1,16
                ;
069F 2917 A          JSR    FORMFD      ;FORM FEED ROUTINE
                 PAGE
06A0            =06B7
                ;
                ; THIS SUBROUTINE OUTPUTS 2 FORM FEEDS
                ; AT THE END OF EACH PRINTOUT AND RESTORES
                ; THE LINE COUNT TO MAXIMUM
                ; IT REPLACES THE 'TYPE' SUBROUTINE
                ; WHICH 'MESG' IN PROM IS NOW USED FOR
                ;
06B7 8014 A FORMFD  LD      0,DEVICE
06B8 F07F A         SKNE    0,ADHSP     ;IS DEVICE PRINTER?
06B9 2101 A         JMP     +2          ;YES
06BA 2105 A         JMP     $END        ;NO
06BB 4C0C A         LI      0,0C        ;FORM FEED
06BC 2C14 A         JSR     @DEVICE     ;OUTPUT FF
06BD 2C14 A         JSR     @DEVICE     ;OUTPUT FF
06BE 4C3C A         LI      0,MAXCNT
06BF B102 A         ST      0,@ALNCNT   ;RESET COUNT
06C0 4D10 A $END    LI      1,16        ;INSTRUCTION REPLACED
06C1 0200 A         RTS     0
06C2 07B0 A ALNCNT  WORD    LNCNT
      0003 A  SPACE 3
06C3            =07A9
                ;
                ; THIS SUBROUTINE COUNTS LINE FEEDS AND
                ; SUBSTITUTES FORM FEEDS AT THE END OF
                ; EACH PAGE
                ; IT REPLACES THE CARD READER SUBROUTINE
                ; 'CRGETC' WHICH IS DISABLED
                ; IF THE CARD READER IS USED THIS ROUTINE
                ; CAN BE SUBSTITUTED FOR THE PRINTER
                ; ROUTINE AND THE PRINTER ROUTINE PLACED
                ; IN PROM
                ;
07A9 F04C A HSPRT1  SKNE    0,H0A       ;LINE FEED?
07AA 7D05 A         DSZ     LNCNT       ;END OF PAGE?
07AB 2103 A         JMP     $OUT        ;NO
07AC 4C3C A         LI      0,MAXCNT
07AD A102 A         ST      0,LNCNT     ;RESET COUNT
07AE 4C0C A         LI      0,0C        ;FORM FEED
07AF 2501 A $OUT    JMP     @PRTC       ;OUTPUT CHAR
07B0 003C A LNCNT   WORD    MAXCNT
07B1 0765 A PRTC    WORD    HSPRT       ;PRINTER ROUTINE
                    PAGE
      0000 A        END
```

```
ADHSP  007F  A    ALNCNT 06C2  A    DEVICE 0014  A
FORMFD 06B7  A    H0A    004C  A    HSPRT  0765  A
HSPRT1 07A9  A    LNCNT  07B0  A    MAXCNT 003C  A
PRTC   07B1  A    SPUTC  0072  A*   STYPE  0079  A*
$END   06C0  A    $OUT   07AF  A

NO ERROR LINES
SOURCE CHECKSUM =A6B1
```

SC/MP-II Microprocessor Highlights

Introduction

The SC/MP-II architecture was designed to meet the needs of designers of low-cost control systems. The following summary of important features and the illustrations showing how to take advantage of these in your design prove our point: *SC/MP-II is an ideal low-cost microprocessor for your control systems.*

Features	User Benefits
• Multiple Addressing Modes • AUTO Indexed Addressing • Logical, Arithmetical, and Control Instructions • Byte Manipulation • Binary and Decimal Arithmetic • Full Range and Relative Jump • Conditional and Unconditional Jump	Applications programs are *easy to write* and are *memory efficient.*
• I/O and Memory Expandability • Expandable Vectored Interrupts • External, Variable-Length Stack	Provides *simplified system design.*
• Bus Control Logic (Hardware)	Allows DMA and *multiprocessor* configuration.
• Separate Serial I/O Port	Allows *serial data transfer* for communication and data acquisition system.
• Three User-Accessible Control Outputs, Two Sense Inputs	Eliminates *external address decoding* and allows *asynchronous sampling* of two discrete inputs.
• Variable "Time Delay" Instruction	Allows *system timing* functions.
• Separate Address and Data Buses	*Eliminates* need for *external address latch.*
• On-Chip Clock Generator	*Eliminates external components.*
• TTL Compatible	*Eliminates special buffers.*
• Single +5 V Supply, Low Power Dissipation (225 mW)	*Saves power.*
• Four STATUS Monitor Flag Outputs	Easy *control logic/debug panel* implementation.

Note: For brevity, the name SC/MP used in text throughout the remainder of this publication refers to the SC/MP-II microprocessing unit.

SERIAL-IN/SERIAL-OUT PORT

SC/MP has a versatile serial-transfer port which uses the EXTENSION register to shift data into and out of serial devices. The serial transfer is accomplished using the SIO Instruction, which shifts data through the EXTENSION register one bit at a time.

The serial I/O port is conveniently used in a variety of applications. ANALOG-TO-DIGITAL CONVERTERS can be implemented simply by using a low-cost comparator to compare an analog voltage to successive digital approximations shifted out by SC/MP as shown in figure 1. The analog signal is converted into an 8-bit digital word and is stored in memory.

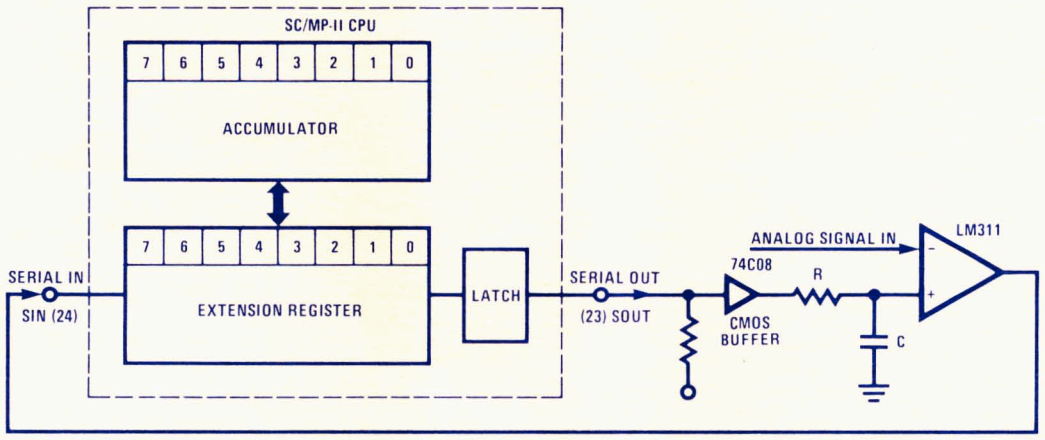


FIGURE 1. SC/MP-II as an Analog to Digital Converter

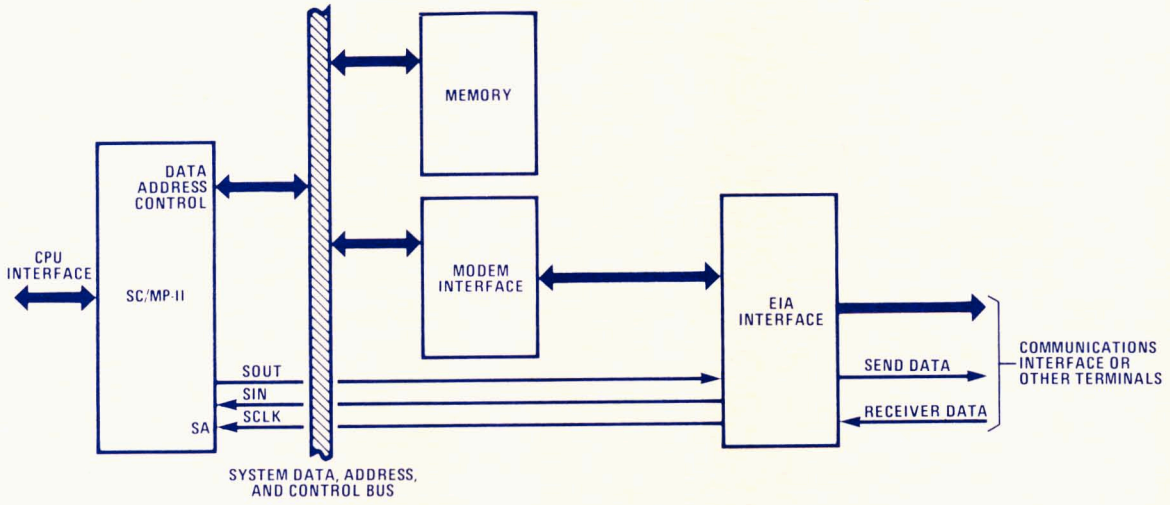


FIGURE 2. SC/MP-II as an Intelligent USRT

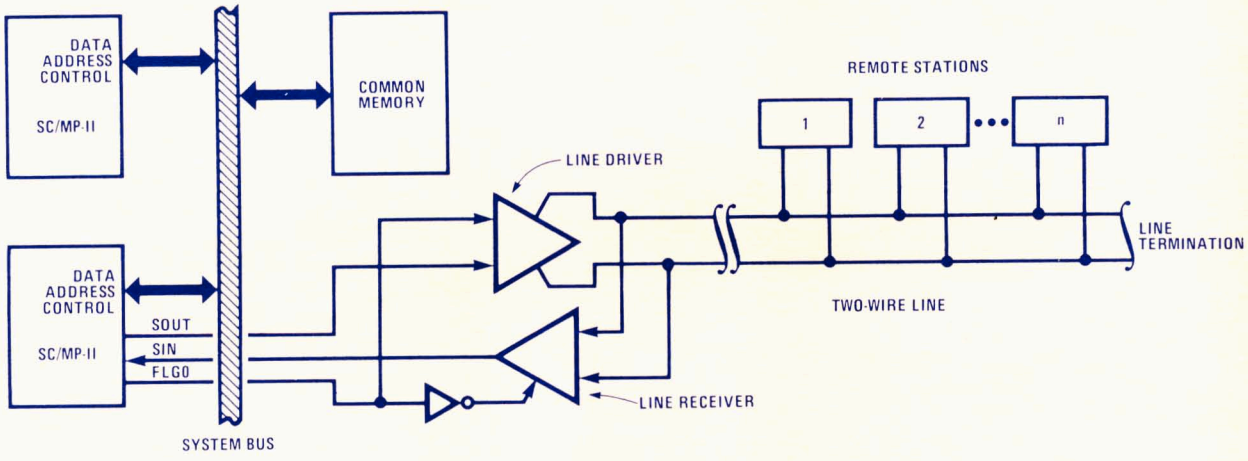


FIGURE 3. SC/MP-II as a Two-Wire Line System Controller

The serial I/O port can also be used as an intelligent USRT capable of operating at up to 4800 baud (see figure 2).

For the two-wire lines used in data acquisition systems, remote peripheral controls, and process controls, SC/MP can be designed as an intelligent controller operating at 9600 baud using standard protocols (see figure 3).

DISTRIBUTED INTELLIGENCE BUS CONTROL LOGIC

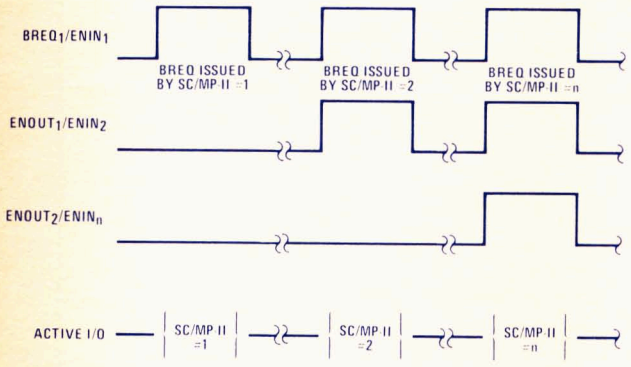
SC/MP-II is specifically designed with multiprocessor bus allocation logic for distributed processing or Direct Memory Access applications. These techniques are often useful in improving system performance. The bus-control logic is explained in the following paragraphs.

Before SC/MP can transfer data, it must have access to the system address/control and data buses. Bus access is controlled by three signals – Bus Request (BREQ), Enable Input (ENIN), and Enable Output (ENOUT). For simple systems, BREQ and ENOUT need not be used, and ENIN can be permanently enabled. Bus access is always controlled by SC/MP, and data transfers from one peripheral to another must go through the processor.

In larger systems, especially those with peripherals that feature high-speed data transfers, Direct Memory Access (DMA) is a method frequently used to effect the fastest data transfers possible between peripherals and memory. Using this technique, data transfers can be directly implemented without involving SC/MP (other than for control functions).

Figure 4 shows a multiprocessor configuration using three SC/MPs. All three SC/MPs share common memory and peripherals and are executing their individual programs.

The three control signals (BREQ, ENIN, and ENOUT) provide both bus-access and priority-select functions. The Enable Input (ENIN) for SC/MP Number 1 is tied to the wire-ANDed BREQ. Thus, if a bus request is issued by the Number 1 processor, it has priority and controls the bus; that is, the input/output cycle for SC/MP Number 1 is active. With SC/MP Number 1 controlling the bus, the Enable Out ($ENOUT_1$) signal is low and other processors in the string are locked out. If both SC/MP Number 2 and SC/MP Number "n" initiate a bus request ($BREQ_2$ and $BREQ_n$ set high) while SC/MP Number 1 is controlling the bus, the following operations occur. $ENOUT_1$ is low until SC/MP Number 1 is finished; then, it goes high. At this time, $ENOUT_1$ and $ENIN_2$ go high; thus, SC/MP Number 2 takes control of the bus. In short, if all processors issue a bus request simultaneously, the string is served on a priority-select basis – SC/MP Number 1 first, SC/MP Number 2 second, SC/MP Number 3 third, and so on.



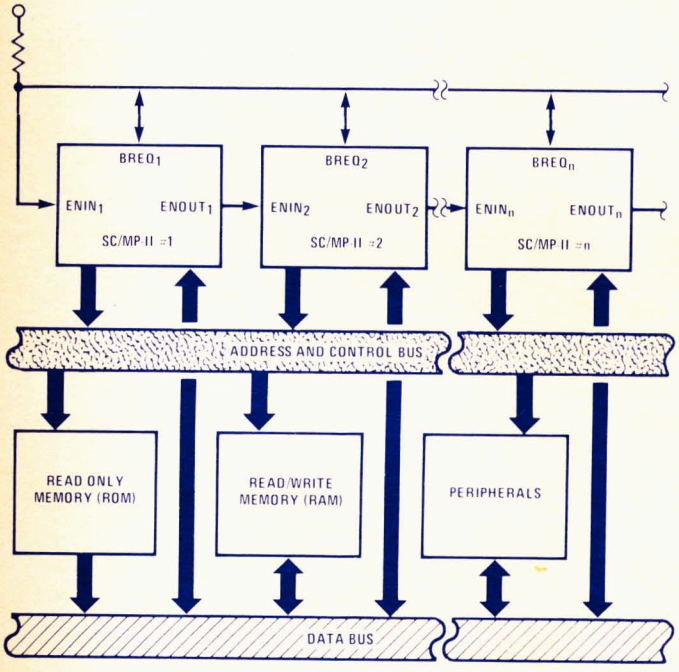


FIGURE 4. Multiprocessor Configuration

Conversely, if SC/MP Number "n" issues a bus request and there are no others awaiting service, $ENIN_n$ is high and the request is granted.

Any one of the SC/MP microprocessors shown in figure 4 can be replaced by a DMA peripheral; the BREQ, ENIN, and ENOUT control signals are used in exactly the same way. Thus, a system designer can economically distribute system functions among several processors and intelligent peripherals. This increases system throughput and eliminates the large hardware/software overhead penalty imposed upon a single processor trying to handle multiple tasks with fast peripherals.

CONDITION SENSING AND CONTROL FLAG LINES

Unlike many other processors which rely on external I/O ports for communication with the outside world, SC/MP has inputs and outputs built into the processor (see figure 5). These are single-bit sense and control lines under the direct control of the programmer, and they are accessed through simple instructions. These I/O lines can be used to directly drive indicators and relays as well as to read process sensors and switches.

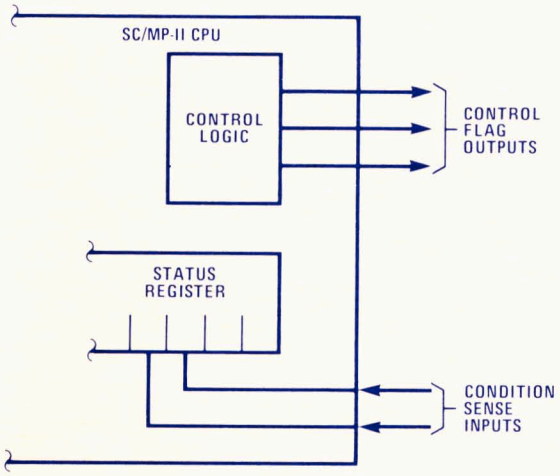


FIGURE 5. SC/MP-II Condition Sensing and Control Flag Lines

Such built-in functions allow the designer to do away with external address decoders and latches in many applications. Additionally, the direct software control that these functions allow means faster programs that require less memory.

The end result for the system designer is lower cost due to less hardware and simpler, easier-to-develop software.

DELAY

Many microprocessor applications call for some type of timing loop. These timing loops generally are inaccurate, take up processor time, and consume program memory space. While the processor is sitting in its timing loop, peripherals on the data bus can access the memory only at a reduced speed. SC/MP has eliminated these problems through the DELAY instruction. The DELAY instruction provides a simple, programmable delay which can be set over a 10,000-to-1 range with crystal accuracy. During the delay time, SC/MP does not require access to the data bus; thus, peripherals or other DMA devices can access memory at full speed. The ability to control

the period of the delay under program control is particularly useful for sequencers, programmable signal generators, and digital phase-locked loops. In these applications, SC/MP's powerful instruction set virtually eliminates the need for additional external hardware.

PARALLEL INPUT/OUTPUT BUSES

SC/MP-II features an 8-bit TRI-STATE® data bus and separate, latched address bus. These features allow the designer to ignore CPU bus loading between I/O cycles and to eliminate external address latches in his system.

SC/MP-II provides all control lines needed to economically build parallel ports onto these buses. Additionally, it provides a series of control signals which can be used in specialized applications to cut system parts count and to provide a higher level of system control. These signals include:

DELAY	Indicates the start of a DELAY instruction.
HALT	Indicates SC/MP-II has executed a HALT instruction.
I-FETCH	Indicates the start of a new instruction fetch.
READ	Indicates a memory fetch.

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AND MUCH MORE . . .

The SC/MP is designed to interface with standard memories and peripheral devices rather than with costly dedicated support chips. Following are some examples of parts and techniques required to expand SC/MP features.

- DM74C151 (8-to-1 MUX) to expand one serial input to 8
- DM74C42 (1-to-8 DEMUX) to expand one serial output to 8
- DM74LS138 (DECODER) to expand one read/write strobe to 8
- AM3705 (ANALOG MUX) to select among 8 analog signals
- DM74C923 (KEYBOARD ENCODER) to directly SCAN a 20-key keyboard
- DM8318 (PRIORITY ENCODER) and DM81LS95 (TRI-STATE® OCTAL BUFFER) to provide 8 prioritized interrupts
- DM74LS138 (DECODER) to encode three output flags to 8
- Software control to provide variable-length stack
- DP8304 (8-bit Bidirectional BUS TRANSCEIVER) to provide buffer and drive capability for 8-bit parallel I/O bus

Dictionary of SC/MP-II Support

A super microprocessor —SC/MP-II. The SC/MP-II is presently available in plastic as well as ceramic package for commercial temperature range of 0° to 70°C. (For industrial and MIL users this is a −40°C to +85°C product.)

Following is the summary and brief description of support products for SC/MP-II.

1) SC/MP-II Retrofit Kit ISP-8K/205
   Allows users easy upgrade of his SC/MP Kit for compatibility evaluation of SC/MP and SC/MP-II.

2) NIBL Kit
   NIBL — National Industrial Basic Language

NIBL is a higher level programming language for SC/MP systems, designed for low speed control applications. Programs written in this language resemble FORTRAN or BASIC programs in which all variables are integers.

- NIBL provides such standard BASIC statements as: LET: PRINT: INPUT: IF/THEN: FOR/NEXT: GOTO: GOSUB: RETURN, etc.
- NIBL allows arbitrary integer arithmetic and logical expressions involving +, -, *, /; AND, OR, NOT; Hex or decimal constants.
- NIBL allows tests for =, >, <, >=, <=, or <> (not =).
- NIBL has several special features which allow the programmer to get close to the machine:
  LINK to machine code subrouting;
  STAT for reading, writing or testing SC/MP status bits;
  '@', an operator which allows reading, writing, or testing of any byte in the address space of SC/MP.

NIBL occupies 4K of ROM and requires at least 2K of RAM, of which all but the first 256 (10) bytes are available for user program. It is totally self-contained as to I/O but is restricted to a 110 baud rate. It will be available as either:

- A set of 8 5214 ROMs ISP-8F/351 — available now
- A set of 2 2316A ROMs ISP-8F/352 — available now

3) 'SUPAK' Line by Line Resident Assembler for LCDS.

SUPAK is a 4K ROM-resident program development utility package for SC/MP LCDS + teletype. It consists of three programs:

- A line-by-line assembler:
  Accepts a program in limited assembly language from keyboard (or paper tape reader) and assembles it directly into RAM
- A paper tape line editor:
  Allows insertion, deletion or replacement of lines of program source code; punches leader or trailer
- A PROM tape punch program:
  Punches the contents of a specified memory range, in BPNF or complemented binary format, onto paper tape

SUPAK requires the LCDS firmware but will run on either a SC/MP OR SC/MP-II LCDS. It will be available as:

- A set of 8 MM5204/MM5214 ROMs
  Part Number ISP-8F/111

4) SC/MP-II CPU Card
   Plug Compatible in LCDS with SC/MP CPU Application Card

   Part Number: ISP-8C/100N (U.S. Card)
   ISP-8C/100NE (Euro Card)

5) SC/MP-II LCDS Retrofit Kit
   Objective is to upgrade SC/MP LCDS in customer location for SC/MP-II development

   LCDS Retrofit Kit consists of:
   a) SC/MP-II CPU Card
   b) Firmware PROM/ROM
   c) Documentation

   Part Number: ISP-8P/301K (U.S. LCDS Retrofit Kit)
   ISP-8P/301KE (Euro LCDS Retrofit Kit)

6) SC/MP-II LCDS
   Factory assembled LCDS to support SC/MP-II based Application Development

   Part Number: ISP-8P/301N (U.S. SC/MP-II LCDS)
   ISP-8P/301NE (Euro SC/MP-II LCDS)

7) SC/MP-II RAM CARD
   SC/MP RAM Application Card compatible RAM Card using higher speed RAM for SC/MP-II based application for 2K x 8 configuration

   Part Number: ISP-8C/002N

For information on items 1, 2, and 3 contact Hash Patel, (408) 737-5175. For information on items 4, 5, 6, and 7 contact Bob Pecotich, (408) 737-6116.

EXTENDED *Temperature Range* SC/MP II

There has been a number of inquiries for SC/MP II operating over extended temperature range.

Guess what? It is here now . .

Our lowest power, N-CH silicon gate technology, 8 bit processor operating on single +5V supply, i.e., SC/MP II is natural for extended temperature range as well as military applications.

The extended temperature range, i.e., –40°C to +85°C, parts will be guaranteed to meet all parameters described in SC/MP II data sheet printed March, 1977.

Call Hash Patel (408) 737-5175 for further information.

SOFTWARE UPDATE

SPROM – IMP-16 – Firmware paper tape generator program: addr 324 should be 6229.

Corrections to the IMP-16 SC/MP Prom Programming Software, SPRSFT

Instructions for Revisions A & B of SPRSFT (Part # 4360943) should be modified to the following values:

addr	data
05BA	2100
05BB	2040
0040	2040
0041	4400
0042	0201

PROGRAMMING TIDBIT

Occasionally, during the execution of a routine, it may be desirable to wait for an interrupt before proceeding through the rest of the routine. The easiest way to do this using PACE is to use the jump (JMP) instruction to put the program in a tight loop that can be exited only by generating an interrupt. The following example illustrates this technique.

```
Main Program
Program
    .
    .
    .
JMP  .–1   ; Await Interrupt
Program (Continued)
    .
    .
    .
    .
```

```
Interrupt Program 1
Program
    .
    .
    .
RTI

Interrupt Program 2
Program
    .
    .
    .
RTI  .–1
```

The .–1 at the JMP instruction causes the Program Counter to be decremented by 1, thereby causing the JMP instruction to be executed, ad infinitum (or until an interrupt is generated). Upon receiving an interrupt, the PC is stored on the stack and the interrupt routine is then executed. To continue with the main program simply execute an RTI, with no displacement value, (see Interrupt Program 1) and the program execution will continue from just below the JMP instruction.

To return to await another interrupt, simply execute an RTI with a displacement value of –1 (see Interrupt Program 2). A –1 will be added to the stored PC on the top of the Stack and the JMP instruction will then be re-executed until another interrupt is generated.

Doug Hall

the Bit • Bucket

Dear Georgia:

Thanks so much for sending me copies of my article in the latest COMPUTE. I was glad you were able to publish it, and look forward to seeing whether or not readers will use and extend its applications.

I recently placed a note in BYTE, the small systems journal for hobbyists, soliciting all hobby users of PACE to get together and share their hints and kinks. So far I've had about several replies and they keep coming in. If we get a viable group formed we will keep you advised of our activities.

Best regards,
Sincerely,

Jock Millenson
5929 Keith Ave.
Oakland, CA 94618

If other PACER users would like to be involved in Jock's club contact him at the above address.

Gentlemen, et al:

I have been receiving COMPUTE since its inception, and consider it a valuable addition to the maelstrom of microprocessor literature with which the industry abounds. Cybertronics has been involved since the beginning as a provider of IC's and supportive hardware, engineering services group, and custom systems house. We have lately been involved heavily in environmental control and energy management applications and the software therewith associated.

I would like to invite your readers to send for our catalogue ($1.00), a 48 page compendium of necessary items, accompanied by a 20 page price list. In addition, I would appreciate the appending of our name and address to the list of "MICROPROCESSOR CONSULTANTS" on the back cover – since we have arrived by default at the state of the art in Louisville, and are busily integrating process control and related micro-based capability into local industry.

Thanks, and keep up the good work!

Steven K. Roberts, President
Cybertronics Incorporated
Microprocessor Systems & Components
312 Production Ct.,
Louisville, KY. 40299,
(502) 499-1551

To: Georgia Marszalek

Solution to possible problems with SC/MP Keyboard Kit.

Immediately after assembly I began experiencing undesired double digit entries and failure to enter a pair of eights and other unexplainable phenomena with the keyboard kit. Several anxious phone calls later to your very service oriented and cooperative field experts, my board looked like it had contracted a fungus with all of the added piggy backed pull-ups and de-coupling caps. The problem stubbornly persisted. Chips were swapped, even the CPU itself. Timing, addressing, the Rom, VCC noise, etc. were carefully scrutinized for any ambiguity and still no solution.

The tip off finally came with the realization that the LEDS were very bright, which meant they were driven hard. Your calculator read out, if it is similar to others with all segs pulled down, should require app 25-35 ma. The 7442 can't handle that kind of current without sacrificing saturation volts (especially with *all* segs firing).

Solution: Replace DM 7442 with DM 7445, (Pin compatible *open collector*).

P.S. Maybe I'm being over elaborate with the solution explanation, but I have spent many frustrating hours localizing the problem, as well as investing in a second CPU chip, and wish to insure that no one else need to. The keyboard kit works great otherwise and have done some promoting of it myself to others.

Bob Bowes
2275 Cooley Place
Pasadena, Calif. 91104

Editor's note: This change is being incorporated in future versions of the Keyboard Kit. Thanks, Bob for your comments.

Attention: Georgia Marszalek, Editor

Gentlemen:

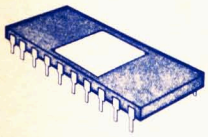
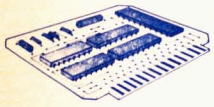
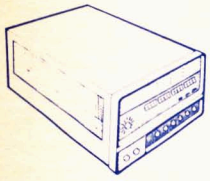
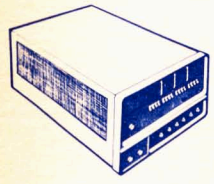
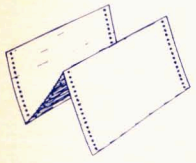
In the March issue of Compute, your answer to a letter published in Bit Bucket stated in part, that you would welcome endorsements of consultants.

Our company, Schwien Engineering, has been working with one of your consultants, Microprocessor Corporation of America for several months. The project has now led to a microprocessor prototype. Throughout this project, the personnel of Microprocessor Corporation of America have been creative and tireless.

They have contributed significantly beyond that required by our contract. I would not hesitate to recommend their services to any prospective user.

John Shaffer
General Manager
Schwien Engineering Inc.
2882 Metropolitan Place
Pomona, CA 91767

PACE 16-Bit Microprocessor Family

	NEW ■	PART NUMBER	DESCRIPTION	AVAILABILITY	PRICE*
					
Chips		IPC-16A/520D	PACE CPU Chip (750ns)	Now	$ 25.00
		DP8300N	Monolithic Bus Transceiver (BTE)	Now	$ 6.55
		DP8301D	Monolithic 8-Bit I/O Port (MILE)	3 Qtr., '77	—
		DP8302J	Monolithic System Timing Element (STE)	Now	$ 7.00
					
Cards		IPC-16C/100	PACE CPU Card	Now	$ 285.00
		IMP-16C/001B	ROM/PROM Socket Card – 1K x 16 Capacity (MM5203Q)	Now	$ 124.00
		IPC-16C/001P	ROM/PROM Card with 1K x 16 (eight) MM5203Q's Inserted	Now	$ 359.00
		IPC-16C/002B	ROM/PROM Socket Card – 2K x 16 Capacity (MM5204Q)	Now	$ 132.00
		IPC-16C/002P	ROM/PROM Card with 2K x 16 (eight) MM5204Q's Inserted	Now	$ 405.00
		IPC-16C/001	RAM Card with 1K x 16 (MM2102) Memory	Now	$ 161.00
	■	IPC-16C/011	LCDS Common Bus RAM Card 1K x 16 (MM2102) Memory	Now	$ 161.00
	■	IPC-16C/012B	LCDS Common Bus ROM/PROM Socket Card with 2K x 16 Capacity (MM5204Q)	Now	$ 132.00
	■	IPC-16C/012P	LCDS Common Bus ROM/PROM Card with 2K x 16 (eight) MM5204Q's Inserted	Now	$ 405.00
		IPC-16C/801	Wire Wrap Prototyping Card	Now	$ 35.00
	■	IPC-16P/802	Common Bus Cable Card ASM	Now	$ 145.00
					
Systems		IPC-16P/108	PACE 8K Development System†	Now	$4,910.00
		IPC-16P/108H	PACE 8K Development System and Heavy Duty† Supply	Now	$5,460.00
		(All Above Include Complete Resident System Software – IPC-16S/901C)			
		IPC-16P/004A	PACE Development System Static RAM Card (4K x 16)	Now	$ 725.00
		IPC-16P/008B	PACE Development System ROM/PROM Socket Card (8K x 16)	Now	$ 370.00
		IPC-16P/008P	PACE Development ROM/PROM Card (8K x 16)	Now	$1,110.00
		IPC-16P/301	PACE Low Cost Development System (LCDS)	Now	$ 585.00
					
Systems		IPC-16P/100	IMP16/PACE System Conversion Kit (CPU Card, PACE Software and Development System Firmware)	Now	$1,000.00
		IPC-16P/805	PROM Programmer for Development System	Now	$ 750.00
		IPC-16P/812	Centronics Printer	Now	$3,700.00
	■	IPC-16P/840	Floppy Disc Operating System: Dual Floppy Disc Drive; Interface Card; ROM Resident Firmware Card; Software on Diskette (requires 12K Memory)	Now	$4,500.00
		IPC-16P/852	Paper Tape Reader (Plessey 1000 cps)	Now	$1,025.00
					
Software		IPC-16S/101C	IMP-16 Based Cross Assembler – 8K Memory Required (paper tape)	Now	$ 100.00
		IPS-16S/102P	Fortran IV Cross Assembler for 16-Bit or Larger Word Computers (Cards)	Now	$ 495.00
		IPC-16S/201C	Basic Interpreter – 8K Memory Required (paper tape)	Now	$ 100.00
		IPC-16S/901C	Resident System Software Package: Source Editor; 4K, 8K and Conversational Assemblers, Absolute and General Loaders; Hardware Diagnostics; plus DEBUG and Utility Software (paper tape)	Now	$ 200.00
			IMP/16 PACE Translator and PACE Cross Assembler Available Through Timeshare Utility Companies		
	■	IPC-16S/902M	Floppy Disc Operating System Software Package on Diskette (copies)	Now	$ 200.00

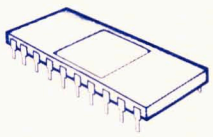
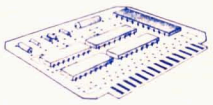
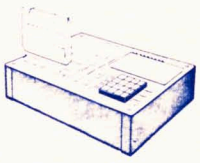
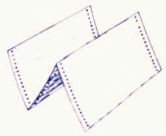
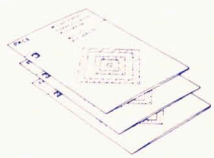
† Other system memory sizes are available. Consult price schedule.

* Prices shown for chips and cards are for quantities of 25 and up. All other prices are for quantities of one and up. Consult National's OEM Price Schedule for other quantity prices.

NOTE: Prices and new product availabilities subject to change without notice; consult your National sales representative or distributor for current prices & product listings.

	NEW ■	PART NUMBER	DESCRIPTION	AVAILABILITY	PRICE*
			Literature		
		IPC-16A/927	Logic Designer's Guide	Now	$ 5.00
	■	IPC-16A/928	System Design Manual	Now	$ 5.00
	■	IPC-16S/969Y	Assembly Language Programming Manual	Now	$ 5.00
	■	IPC-16P/840Y	PACE DOS Users Manual	Now	$ 5.00
	■	IPC-16S/201Y	PACE Basic Users Manual	Now	$ 5.00
	■	IPC-16P/301Y	PACE LCDS Users Manual	Now	$ 5.00
	■	IPC-16P/108Y	PACE Development System Users Manual	Now	$ 10.00
			IPC-16A/520 Data Sheet	Now	FREE
			DP8300N Data Sheet	Now	FREE
			DP8302J Data Sheet	Now	FREE

SC/MP 8-Bit Microprocessor Family

	NEW ■	PART NUMBER	DESCRIPTION	AVAILABILITY	PRICE*
			**Chips**		
		ISP-8A/500D	SC/MP CPU Chip	Now	$ 15.00
	■	ISP-8A/600D/N	SC/MP-II CPU Chip	Now	$ 15.00/12.00
	■	DP8304D	Bus Transceiver	Now	$ 5.70
	■	ISP-8A/650D/N	128 x 8 RAM with 16 Prog. I/O Ports	3 Qtr., '77	—
	■	INS2656	ROM/RAM/I/O	3 Qtr., '77	—
	■	MM5235	8K x 8 ROM	3 Qtr., '77	—
			**Cards**		
		ISP-8C/100	SC/MP CPU Card with 256 x 8 RAM, 512 x 8 ROM/PROM Socket	Now	$238.00
	■	ISP-8C/100N	SC/MP-II CPU Card with 256 x 8 ROM/PROM Socket	Now	$238.00
		ISP-8C/002N	RAM Card (2K x 8 Static Memory RAM, 512 x 8)	Now	$152.00
		ISP-8C/004B	PROM/ROM Socket Card – 4K x 8 (accepts 8 MM5204Q/MM5214)	Now	$119.00
		ISP-8C/004P	PROM/ROM Memory Card – 4K x 8 (with 8 blank MM5204Q)	Now	$499.00
		IPC-8C/801	Wire Wrap Prototyping Card	Now	$ 35.00
	■	ISP-8P/802	Common Bus Cable Card ASM	Now	$145.00
			**Systems**		
	■	ISP-8P/301K	SC/MP-II LCDS Retrofit Kit	Now	$199.00
		ISP-8P/301	SC/MP Low-Cost Development System (includes CPU Application Card)	Now	$499.00
	■	ISP-8P/301N	SC-MP-II Low-Cost Development System (includes CPU Application Card)	Now	$499.00
		ISP-8K/200	SC/MP Kit – An Introductory Package for New Users	Now	$ 99.00
	■	ISP-8K/205	SC/MP-II Retrofit Kit	Now	$ 18.50
		ISP-8K/220	SC/MP Kit Fully Assembled and Tested	Now	$125.00
		ISP-8K/400	SC/MP Keyboard Kit – Hex Keyboard/Display	Now	$ 95.00
			**Software**		
		ISP-8S/100C	IMP-16 Based Cross Assembler – 4K (paper tape)	Now	$150.00
		ISP-8S/101C	IMP-16 Based Macro Cross Assembler – 8K (paper tape)	Now	$150.00
		ISP-8S/103C	PACE-P Based Macro Cross Assembler – 8K (paper tape)	Now	$150.00
		ISP-8S/102P	Fortran IV Cross Assembler for 16-Bit Word or Larger Computers	Now	$495.00
	■	ISP-8F/111	SC/MP-II LCDS Firmware Assembler Package (SUPAK): Line Assembler, Source Editor, P/N Tape Generator (in 8 MM5214 ROMs)	Now	$300.00
	■	ISP-8F/351	SC/MP-II National Industrial Basic Lang. (NIBL) Firmware (in 8 MM5214 ROMs)	Now	$260.00
	■	ISP-8F/352	SC/MP-II NIBL Firmware (in 2 MM2316A ROMs)	Now	$ 85.00
			**Literature**		
		ISP-8S/994Y	SC/MP Assembly Language Programming Manual	Now	$ 10.00
	■		SC/MP-II Brochure	Now	FREE
		4200079A	SC/MP – Technical Description	Now	$ 3.00
		420305239-001A	SC/MP Applications Handbook	Now	$ 5.00
	■		SC/MP-II Data Sheet (ISP-8A/600)	Now	FREE
	■		SC/MP Data Sheet (ISP-8A/500)	Now	FREE

* Prices shown for chips and cards are for quantities of 25 and up. All other prices are for quantities of one and up. Consult National's OEM Price Schedule for other quantity prices.
NOTE: Prices and new product availabilities subject to change without notice; consult your National sales representative or distributor for current prices & product listings.

Support Devices and Literature

	NEW ■	PART NUMBER	DESCRIPTION	AVAILABILITY	PRICE*
Universal Interface		DP8212N/J	8-Bit I/O Port	Now	$ 3.30/3.90
		INS8255D	Programmable Parallel Interface	Now	$12.80
		81LS95/98	Tri-State® Octal Buffers	Now	$ 7.70
		DM8542N	Quad I/O Register	Now	$ 5.60
		MM74C173/174N	4-Bit CMOS Latches	Now	$ 1.26
		DM74173/174N	4-Bit Tri-State® Latches	Now	$ 3.20/ 2.48
		DM74LS173/174N	4-Bit Low Power Schottky Latches	Now	$ 3.40/ 1.65
		DM8546N	Tri-State® 8-Bit Universal I/O Shift Reg	Now	$ 4.80
		LM555CN/556CN	Interval Timer	Now	$ .66/ 1.15
		DM74147N/748N	Priority Encoder (Interrupt/DMA Control)	Now	$ 4.00/ 2.48
		DS8833N	Tri-State® Quad Bus XCVR	Now	$ 2.35
		DS8835N	Bi-Directional Bus Driver Inv.	Now	$ 2.35
		DM74LS138N	1-of-8 Binary Decoder (replaces Intel 8205)	Now	$ 1.55
		DP8301D	Monolithic 8-Bit I/O Port	Now	$ 7.00
	■	DP8304	Octal Bus Driver	Now	$ 5.30
	■	INS8253	Programmable Timer	4 Qtr., '77	—
	■	INS8257	Programmable DMA Controller	4 Qtr., '77	—
	■	INS8259	Programmable Interrupt Controller	4 Qtr., '77	—
	■	BP8350	Programmable CRT Controller	4 Qtr., '77	—
Human Interface		MM74C922/3	16 & 20-Key Keyboard Encoders	Now	$ 4.55/ 4.65
		MM5740AAX/N	90-Key Keyboard Encoder	Now	$14.40
		DM8544N	Tri-State® Quad Switch Debouncer	Now	$ 1.20
		DS8859, 69N	Hex Latch/Led Driver	Now	$ 1.50
		CD4511CN	7-Segment Latch Decoder Driver	Now	$ 2.76
		DS8692, 3, 4	Seiko Printer Interface Set	Now	Contact Factory
		DM8678XXX/N/J	CRT Character Generator	Now	$17.60/20.40
Instrument & Machine Interface		DM8334N	8-Bit Bit-Addressable Latch	Now	$ 4.00
		ADC0800PCN	8-Bit A-to-D Converter	Now	$ 9.60
		ADC1210, 11	CMOS A-to-D Converter (12/10 Bit)	Now	$33.85
		DAC1200, 02CN	12-Bit D-to-A Converter (Binary/BCD)	Now	$33.00
		CD4051CN	8-Ch. Analog Mux/Demux	Now	$ 1.26
		DAC1201, 03CN	10-Bit D-to-A Converter	Now	$27.00
Memory with Input/Output	■	INS2656	ROM/RAM/I/O	3 Qtr., '77	—
		ISP-8A/650D/N	128 x 8 RAM with 16 Prog I/O Port	3 Qtr., '77	—
RAMs		MM2114	1k x 4 Static RAM	3 Qtr., '77	—
		MM5257	4k x 1 Static RAM	3 Qtr., '77	—
		MM2102/2N	1k x 1 Static RAM	Now	$ 2.80
		MM5269N	256 x 4 Static RAM with Latched Inputs	Now	$ 3.85
		MM5270, 80D	4k x 1 Dynamic RAMs	Now	$14.40/18.00
		MM74C920D	1k x 1 CMOS Static RAM	Now	$14.60
		MM2111-2N	256 x 4 Static RAM, Common I/O	Now	$ 3.85
		MM2102AN-4	1k x 1 Static RAM, 450ns	Now	$ 3.00
ROMs		MM5214N	512 x ROM	Now	$23.00
		MM5242N	1k x 8 NMOS ROM	Now	$15.00
		MM2316A	2k x 8 ROM	Now	Contact Factory
		DM85S28XXX/J/N	1k x 8 ROM (Pinout Similar to MM2708)	Now	$48.88/46.35
	■	MM5235	8K x 8 ROM	3 Qtr., '77	—
PROMs		DM2704N	512 x 8 PROM with 2708 Pinouts	Now	$21.25
		MM5204Q	512 x 8 Erasable PROM	Now	$35.40
		MM1702AQ	256 x 8 Erasable PROM	Now	$28.45
		MM2708Q	1k x 8 Erasable PROM	Now	Contact Factory
		DM87S222N	256 x 8 PROM with Latched Inputs (20 pin DIP)	3 Qtr., '77	—
		DM74S472N	512 x 8 PROM (20 pin DIP)	3 Qtr., '77	—
		DM87S296N	512 x 8 PROM	Now	$21.25
Communications		MM5307AA/N	Baud Rate Gen./Prog. Real Time Clock	Now	$14.00
		MM5303N	UART	Now	$ 7.20
		INS57101	Asynchronous Communication Element	3 Qtr., '77	—
		INS8251	Programmable Communications Interface	3 Qtr., '77	—
	■	INS1671	Astro Communications Interface	Now	—
	■	INS1771-1	Floppy Disc Controller	Now	—
	■	INS2651	USART/Baud Rate Gen.	3 Qtr., '77	—
	■	INS2652	Multi Protocol Comm. (SDLC)	3 Qtr., '77	—
Literature			TTL Products Catalog	Now	$ 4.00
			Interface Products Catalog	Now	$ 4.00
			Special Function Products Catalog	Now	$ 3.00
			Memory Products Catalog	Now	$ 3.00
	■		Microprocessor Full Spectrum Brochure	Now	FREE
	■		Microprocessor Cards & System Brochure	Now	FREE
	■		Microprocessor Training Brochure	Now	FREE

* Prices shown for chips and cards are for quantities of 25 and up. All other prices are for quantities of one and up. Consult National's OEM Price Schedule for other quantity prices.
NOTE: Prices and new product availabilities subject to change without notice; consult your National sales representative or distributor for current prices & product listings.

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*Applications Engineer Available

Telecommunications Circuits

A new catalog of microprocessors and integrated circuits designed for telecommunications applications, is now available from National.

The booklet contains descriptions, data, and applications notes, and diagrams of twelve different subsystems product lines that are of particular importance to manufacturers and users of modern telecommunications systems equipment.

The booklet is available without charge from National Semiconductor, 2900 Semiconductor Drive, Santa Clara, California 95051, and from National's local sales offices.

TRANSLATION PLEASE!

Occasionally we get letters or COMPUTE orders where the address is difficult to read. When we translate these to the envelope labels with your library requests or orders they are returned because the postal service cannot find you. If at all possible please use your mailing label on all correspondence to the user group, print legibly or type your name and address. Thanks a lot.

SCHEDULE OF MICROPROCESSOR RESIDENT TRAINING PROGRAMS

	EASTERN TRAINING CENTER	WESTERN TRAINING CENTER
MICROPROCESSOR FUNDAMENTALS	SEPTEMBER 19-22 OCTOBER 17-20 JANUARY 9-12 FEBRUARY 6-9 APRIL 3-6 MAY 1-4	AUGUST 22-25 SEPTEMBER 19-22 OCTOBER 17-20 FEBRUARY 6-9 MARCH 6-9 APRIL 3-6
SC/MP APPLICATIONS	AUGUST 1-4 SEPTEMBER 26-29 OCTOBER 24-27 JANUARY 16-19 FEBRUARY 13-16 APRIL 10-13 MAY 8-11	AUGUST 1-4 AUGUST 29-SEPTEMBER 1 SEPTEMBER 26-29 OCTOBER 24-27 FEBRUARY 13-16 MARCH 13-16 APRIL 10-13 MAY 1-4
PACE APPLICATIONS	AUGUST 8-11 OCTOBER 3-6 OCTOBER 31-NOVEMBER 3 JANUARY 23-26 FEBRUARY 20-23 APRIL 17-20 MAY 15-18	AUGUST 8-11 SEPTEMBER 5-8 OCTOBER 3-6 OCTOBER 31-NOVEMBER 3 FEBRUARY 20-23 APRIL 17-20 MAY 8-11
ADVANCED PROGRAMMING	OCTOBER 10-13 FEBRUARY 27-MARCH 2	NOVEMBER 7-10
8080/PERIPHERALS	AUGUST 22-25 DECEMBER 5-8 MARCH 27-30	JANUARY 30-FEBRUARY 2 MAY 22-25

POWER TRANSISTOR DATA BOOK

A new data book and power catalog that details more than one hundred discrete power semiconductor products is now available from National.

This is the first catalog to describe National's complete line of power transistors, which include four plastic packages: TO-126, TO-202, TO-220 and the innovative 92 Plus package, as well as the standard (metal) TO-3 package.

The book provides access to all specifications, and is cross-indexed with part number to process conversion for all the devices. The reference guide allows the engineer to pinpoint the voltage current and package he needs in the simplest way.

The 152 page data book is available from National Semiconductor Corporation, Marketing Services, 2900 Semiconductor Drive, Santa Clara, California 95051, $3.00 postpaid.

HEXADECIMAL TO DECIMAL DISPLACEMENT TABLE

-HEX	DEC	HEX	-HEX	DEC	HEX	-HEX	DEC	HEX	-HEX	DEC	HEX
FF	01	01	DF	33	21	BF	65	41	9F	97	61
FE	02	02	DE	34	22	BE	66	42	9E	98	62
FD	03	03	DD	35	23	BD	67	43	9D	99	63
FC	04	04	DC	36	24	BC	68	44	9C	100	64
FB	05	05	DB	37	25	BB	69	45	9B	101	65
FA	06	06	DA	38	26	BA	70	46	9A	102	66
F9	07	07	D9	39	27	B9	71	47	99	103	67
F8	08	08	D8	40	28	B8	72	48	98	104	68
F7	09	09	D7	41	29	B7	73	49	97	105	69
F6	10	0A	D6	42	2A	B6	74	4A	96	106	6A
F5	11	0B	D5	43	2B	B5	75	4B	95	107	6B
F4	12	0C	D4	44	2C	B4	76	4C	94	108	6C
F3	13	0D	D3	45	2D	B3	77	4D	93	109	6D
F2	14	0E	D2	46	2E	B2	78	4E	92	110	6E
F1	15	0F	D1	47	2F	B1	79	4F	91	111	6F
F0	16	10	D0	48	30	B0	80	50	90	112	70
EF	17	11	CF	49	31	AF	81	51	8F	113	71
EE	18	12	CE	50	32	AE	82	52	8E	114	72
ED	19	13	CD	51	33	AD	83	53	8D	115	73
EC	20	14	CC	52	34	AC	84	54	8C	116	74
EB	21	15	CB	53	35	AB	85	55	8B	117	75
EA	22	16	CA	54	36	AA	86	56	8A	118	76
E9	23	17	C9	55	37	A9	87	57	89	119	77
E8	24	18	C8	56	38	A8	88	58	88	120	78
E7	25	19	C7	57	39	A7	89	59	87	121	79
E6	26	1A	C6	58	3A	A6	90	5A	86	122	7A
E5	27	1B	C5	59	3B	A5	91	5B	85	123	7B
E4	28	1C	C4	60	3C	A4	92	5C	84	124	7C
E3	29	1D	C3	61	3D	A3	93	5D	83	125	7D
E2	30	1E	C2	62	3E	A2	94	5E	82	126	7E
E1	31	1F	C1	63	3F	A1	95	5F	81	127	7F
E0	32	20	C0	64	40	A0	96	60	80	128	80

We would like to thank whoever sent in the above table; however, we lost the name and address.
Sorry about that.

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SC/MP II COMPATIBILITY

There was a short article in the May 1977 issue of COMPUTE announcing the SC/MP-II Microprocessor Chip. The article stated that the SC/MP and SC/MP-II chips are software pin-out compatible. This is not entirely true. The two chips are software compatible except for timing delays. Since SC/MP-II runs much faster than SC/MP, any timing delays in a SC/MP program must be modified before the program will run correctly on a SC/MP-II. SC/MP and SC/MP-II have the same pinouts except the power pins. The differences are as follows:

SC/MP		SC/MP-II	
Pin	Signals	Pin	Signals
20	$+5(V_{SS})$	20	GND
40	$-7(V_{GG})$	40	$+5(V_{CC})$

In addition the active input level for the following signals has changed from active low to active high:

SC/MP			SC/MP-II		
Pin	Signal	Active	Pin	Signal	Active
3	ENIN	low	3	ENIN	high
4	ENOUT	low	4	ENOUT	high
5	BREQ	low	5	BREQ	high

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